UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: July 2017

Module Number: EE5208 **Module Name: Electronic Circuit Design**

[3 Hours]

[Answer **all questions**, each question carries 12.5 marks]

Q1 a) Explain why capacitors are considered as passive elements.

[1.0 Mark]

b) A capacitive voltage divider circuit is shown in Figure Q1 b). Assume, $C_1 = 100\ \mu F$ and the tolerance values for both capacitors as 5%. Input voltage $V_{in} = 100$ V. Select a suitable value for C_2 from E12 series such that $55\ V \leq V_0 \leq 65\ V$.

[3.0 Marks]

c) A typical Zener regulator circuit is shown in Figure Q1 c). The tolerance of R is ± 5%. Input voltage $V_{in} = 15\ V \pm 5\%$ and the output voltage $V_o = 8\ V \pm 5\%$.
You are given two Zener diodes having the rated values as shown in Table Q1 b). The maximum load current should be kept to 150 mA while the minimum to 0 mA.

i) Stating any assumptions you make, select a suitable zener diode from Z1 and Z2.

ii) Determine suitable values for R from E12 series.

Table Q1 b)

Zener Diode	Rated Voltage	Rated Power
Z1	8.5 V	2 W
Z2	8.5 V	1 W

[6.0 Marks]

d) A Zener diode regulator circuit is shown in Figure Q1 d). Zener voltage $V_Z = 10$ V and the tolerance of R_s is ± 5%.
Determine the value range of R_s using the parameters given in Table Q1 d) to ensure that the Zener diode remains in the breakdown region.
Hint:
You can formulate two worst case scenarios based on the following condition,

$$I_{Z\,min} \leq I_Z \leq I_{Z\,max}$$

Table Q1 d)

Parameter	Minimum	Maximum
V_{in}	15 V	20 V
I_Z	5 mA	100 mA
I_L	0 mA	20 mA

[2.5 Marks]

Q2 a) A PCB (Printed Circuit Board) provides both a physical structure for mounting and holding electronic components and the electrical interconnection between components.

i) Give two advantages of PCBs.
ii) Classify PCBs according to layers of wiring.
iii) Give two mechanisms to provide interconnections for double sided non-plated through hole with relevant sketches.
iv) State what is meant by "Via" in double sided PCBs.
v) List the basic PCB design steps.

[6.0 Marks]

b) State the three basic rules defined for PCB layout design.

[1.5 Marks]

c) Briefly explain two drilling problems.

[2.0 Marks]

d) The process of removing metal from the surface of a PCB by chemical dissolution is called Etching.

i) State four etching solutions.
ii) Compare immersion etching and bubble etching with relevant sketches.
ii) State what is meant by "Under-cut" in etching.

[3.0 Marks]

Q3 a) What is the function of a filter?

[0.5 Marks]

b) A passive low pass filter circuit consisting of a resistor of 10 kΩ in series with a capacitor of 22 nF is connected across a 12 V sinusoidal supply. Determine the following.

i) output voltage at 100 Hz
ii) output voltage at 10 kHz

[4.0 Marks]

c) Give first order high pass filter design circuits for both inverting and non-inverting cases and state the transfer functions for them.

[2.0 Marks]

d) Design a practical fifth order unity-gain Butterworth low pass filter with cutoff frequency $f_c = 150$ kHz using Sallen-Key topology.
Capacitance values for the filters are shown in Table Q3 d). Design each partial filter and draw it as a combination by specifying the available capacitor values and the resistor values. Make necessary assumptions if required.

Hint:
You may refer Table Q3 d_1) and Table Q3 d_2) to find the resistor and capacitor values respectively.

Table Q3 d)

Type	a_i	b_i	Capacitance
Filter 1	$a_1 = 1.0000$	$b_1 = 0.0000$	33 nF
Filter 2	$a_2 = 1.6180$	$b_2 = 1.0000$	750 pF
Filter 3	$a_3 = 0.6180$	$b_3 = 1.0000$	130 pF

[6.0 Marks]

Q4 a) i) State 3 differences between a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and a BJT (Bipolar Junction Transistor).

ii) Sketch the structure of a depletion type N-channel MOSFET showing the DC biasing for normal operation. (Clearly indicate the depletion region and the channel of conduction)

iii) Explain why self-bias is impossible with enhancement type N-channel MOSFETs.

iv) Reproduce the enhancement type N-channel MOSFET drain and transfer characteristics and indicate the different regions of the curve.

[4.0 Marks]

b) The enhancement type N-channel MOSFET in the circuit shown in Figure Q4 b) has the following parameters.

$V_T = 2$ V, $\beta = 0.6 \times 10^{-3}$ A/V^2 and $r_d = 90$ kΩ

i) Verify that the MOSFET is biased in its active region.

ii) Determine the Transconductance (g_m) of the MOSFET.

iii) Draw the small signal ac equivalent circuit and find the overall voltage gain (V_L/ V_s).

iv) Redraw the small signal ac equivalent circuit if source resistor (1 kΩ) is un-bypassed.

[7.0 Marks]

c) i) Explain with relevant sketches, how an enhancement MOSFET can be used as a nonlinear resistor.

ii) If the drain characteristic of such a MOSFET is given by,

$$I_D = 0.5\beta(V - V_T)^2, \quad V > V_T$$
$$I_D = 0, \quad V \le V_T$$

show that the small signal ac resistance is, $r = \dfrac{1}{\sqrt{2\beta I}}$

where I denotes the current.

[1.5 Marks]

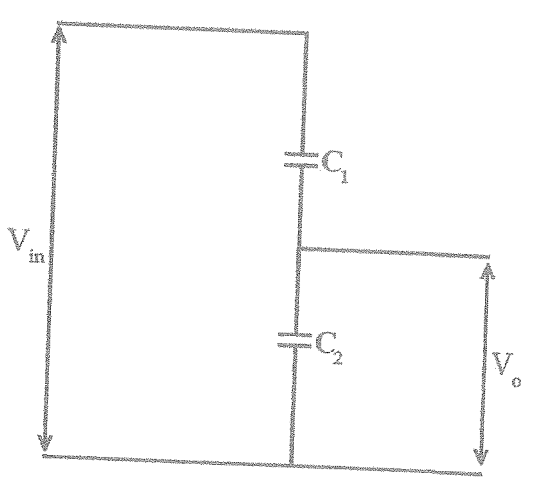

Figure Q1 b)

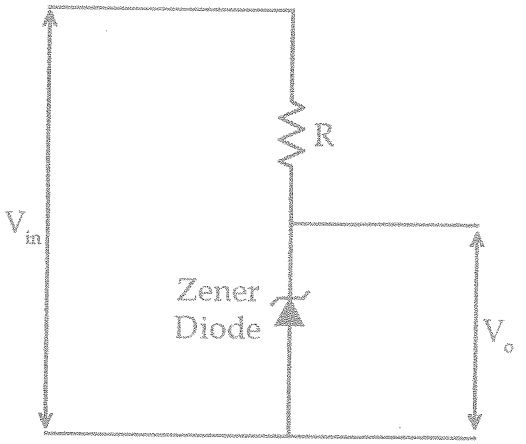

Figure Q1 c)

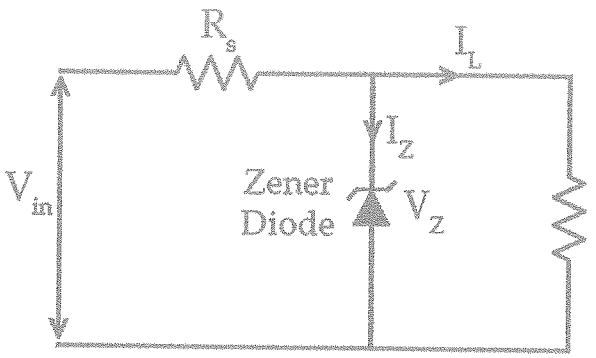

Figure Q1 d)

Table Q3 d_1): E96 Resistor Series

100	102	105	107	110	113	115	118	121	124	127	130
133	137	140	143	147	150	154	158	162	165	169	174
178	182	187	191	196	200	205	210	215	221	226	232
237	243	249	255	261	267	274	280	287	294	301	309
316	324	332	340	348	357	365	374	383	392	402	412
422	432	442	453	464	475	487	499	511	523	536	549
562	576	590	604	619	634	649	665	681	698	715	732
750	768	787	806	825	845	866	887	909	931	953	976

Table Q3 d_2): Capacitor Letter Codes

Picofarad (pF)	Nanofarad (nF)	Microfarad (uF)	Code	Picofarad (pF)	Nanofarad (nF)	Microfarad (uF)	Code
10	0.01	0.00001	100	4700	4.7	0.0047	472
15	0.015	0.000015	150	5000	5.0	0.005	502
22	0.022	0.000022	220	5600	5.6	0.0056	562
33	0.033	0.000033	330	6800	6.8	0.0068	682
47	0.047	0.000047	470	10000	10	0.01	103
100	0.1	0.0001	101	15000	15	0.015	153
120	0.12	0.00012	121	22000	22	0.022	223
130	0.13	0.00013	131	33000	33	0.033	333
150	0.15	0.00015	151	47000	47	0.047	473
180	0.18	0.00018	181	68000	68	0.068	683
220	0.22	0.00022	221	100000	100	0.1	104
330	0.33	0.00033	331	150000	150	0.15	154
470	0.47	0.00047	471	200000	200	0.2	254
560	0.56	0.00056	561	220000	220	0.22	224
680	0.68	0.00068	681	330000	330	0.33	334
750	0.75	0.00075	751	470000	470	0.47	474
820	0.82	0.00082	821	680000	680	0.68	684
1000	1.0	0.001	102	1000000	1000	1.0	105
1500	1.5	0.0015	152	1500000	1500	1.5	155
2000	2.0	0.002	202	2000000	2000	2.0	205
2200	2.2	0.0022	222	2200000	2200	2.2	225
3300	3.3	0.0033	332	3300000	3300	3.3	335

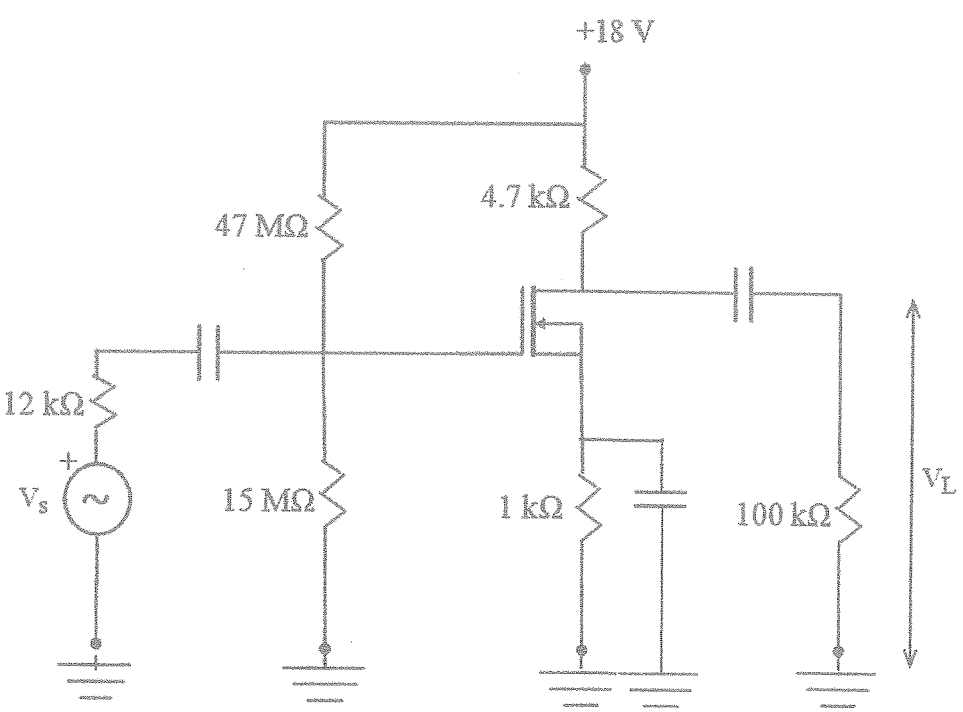

Figure Q4 b)