UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5, Examination in Engineering, July 2016

Module No: EE5201 **Module Name: Computer Architecture**

[1 hour 45 Minutes]

[Answer all questions. Each question carries 10 marks]

Part II

Q1. a) Why access time of SRAM is shorter than of DRAM? [2 Marks]

b) Give the internal organization of 32MBit DRAM organized in an 8-bit Chip Array in a block diagram. Indicate and name major components and signals of external buses. [2 Marks]

c) What is the main advantage of N-bit Chip Array organization in terms of computer organization aspects? Describe by using a numerical example. [2 Marks]

d) Describe the Read and Write Operations of DDR-SDRAM by using appropriate timing diagram. [2 Marks]

e) i. Find the check bits of Hamming Error Correction Code for the data bits 1101.

ii. Propose an error correction mechanism for main memory read/write operations, by using an apprpriate block diagram.

[2 Marks]

Q2. a) Draw the timing diagram for a CPU pipeline having 6 data path stages;
FI - Fetch Instruction, DI - Decode Instruction, CO - Calculate Operand
FO - Fetch Operand, EI - Execute Instruction, WO - Write Operand. (Assume no hazards occur). [2 Marks]

b) Redraw the above timing diagram to show the effect of Control Hazard. [2 Marks]

c) Derive equation for Speed-up $S_{k,n}$ as a function of n - number of executed instructions, and k - number of stages of the pipeline, assuming ideal conditions (i.e. no hazards). Discuss the effects of increasing k and n. [2 Marks]

d) In a CPU of 5 stage pipeline, first 2 stages take 30ns each while next 3 stages take 50ns each. Assuming no hazards occurring, calculate the speed-up of the CPU for a program of 20 instructions. [2 Marks]

e) A non-pipelined CPU has a clock rate of 2.5GHz and an average CPI (Cycles Per Instruction) of 4. An upgrade to the CPU introduces a 5-stage pipeline. However, due to the internal pipeline delays, the clock rate of the new CPU has to be reduced to 2GHz.

i. What is the Speed-up for a typical program?

ii. What are throughputs in MIPS (Million Instructions per Second) for each processor?

[2 Marks]

Q3. a) What is the purpose of using a memory hierarchy in computer architecture? [2 Marks]

b) Describe the meanings of Cache and Main Memory mapping parameters; Word, Block, Line and Tag. You may use a block diagram to explain. [2 Marks]

c) Compare and contrast Cache mapping functions; Direct, Associative and Set-Associative mapping. [2 Marks]

d) Consider the 16 MByte of flat memory which is connected to the CPU through 64KBytes of Cache memory, having Blocks of size 4 Words. Size of a Word is 1 Byte.

i. Draw a block diagram of Cache and Main Memory indicating the direct mapping parameters; Word, Block, and Tag.

ii. What is the format of the read address for Direct, Associative and Set-Associative mapping?

[2 Marks]

e) Explain two Cache Coherence algorithms suitable for a single core machine. [2 Marks]