UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 2 Examination in Engineering: November 2016

Module Number: EE2202 **Module Name: Introduction to Electronic Engineering**

[Three Hours]

[Answer **all questions**, each question carries **10 marks**]

All notations have their usual meanings.

Q1 a) Figure Q1 a) shows three BJT (Bipolar Junction Transistor) configurations.

i) Identify the configurations.

ii) Sketch the output characteristics of the configurations, clearly labeling the axes and their units.

iii) Identify the operating regions saturation, active and cut-off in your sketches for part ii).

[5 Marks]

b) Figure Q1 c) shows the bias circuits for two BJT configurations.

i) Find the bias points for the two cases.

ii) Identify the configuration for the BJT to act as a switch.

iii) Re-design the bias circuit for the BJT to act as a switch and explain its operation.

[5 Marks]

Q2 a) i) State the purpose of bias in a transistor amplifier.

ii) When a transistor amplifier is biased and a sinusoidal signal is input, the output of the positive half of the signal is found to be clipped. Explain the reason for this.

[3 Marks]

b) i) Figure Q2 b) shows a BJT amplifier connected to a source V_s with the output open. Give the AC equivalent circuit of the amplifier and calculate the voltage gain A_v of the amplifier. The current gain is β.

ii) The amplifier in Figure Q2 b) is now connected to a source V_s with source resistance r_s and a load resistance R_L. Give the circuit diagrams and calculate the overall voltage and current gains.

[4 Marks]

c) Figure Q2 d) shows an Emitter Follower with a Silicon BJT with $\beta = 100$. Determine

i) the input resistance r_{in}

ii) the voltage gain A_v

[3 Marks]

Q3 a) i) Give the circuit symbols for an N - JFET and a P - JFET.

ii) Sketch the structure of a biased N-type JFET and show the terminals, the channel and the biasing voltage sources V_{DS} and V_{GS}.

iii) Sketch the formation of the depletion regions for

I) $V_{DS} = 0$, $V_{GS} \neq 0$

II) $V_{GS} = 0$, $V_{DS} \neq 0$

III) Explain the difference in the shape of the depletion regions in parts I) and II).

iv) An N – JFET has a pinch-off voltage $|V_P| = 4$ V and a saturation current $I_{DSS} = 12$ mA.

I) For $V_{GS} = -1$ V, at what value of V_{DS} will pinch-off take place?

Note: $V_{DS} = V_{GS} - V_P$

II) At what value of V_{GS} will $I_D = 4$ mA

Note: $I_D = I_{DSS}\,(1 - V_{GS}/V_P)^2$

[5 Marks]

b) i) Sketch the structure of an N – type biased depletion type MOSFET and show the terminals, the channel and the bias voltage sources V_{DS} and V_{GS}.

ii) The depletion type MOSFET can also be used in the enhancement mode. Sketch the depletion MOSFET drain characteristics for operation in the depletion and enhancement modes.

iii) Sketch the structure of an N-type enhancement type MOSFET and explain how the channel is formed.

[5 Marks]

Q4 a) i) Draw the block diagram of a sequential circuit and name all the blocks.

ii) State the main difference between combinational and sequential circuits?

iii) What is meant by *state* of a sequential circuit?

iv) Name the two main types of sequential circuits and briefly explain them.

v) Briefly explain the synchronous sequential logic systems.

[5 Marks]

b) You are required to analyze the digital circuit given in Figure Q4. In the circuit a special clocked PQ flip-flop (FF) is used. The PQ FF has two inputs P and Q and it operates as follows.

- If PQ = 00, the next state of the FF output is 1.
- If PQ = 01, the next state of the FF output is the same as present.
- If PQ = 10, the next state of the FF output is the complement of present.
- If PQ = 11, the next state of the FF output is 0.

i) Derive the characteristic table of the PQ FF.

ii) The input functions of the FF are given in (1) and (2) below. Simplify the input functions using Karnaugh maps.

$$P_A = (\bar{x}y + x)(zA + z\overline{A}) + \overline{(x + y + x\bar{y})}(\overline{z\overline{A}} + z\bar{A}) + xy\bar{z}A \quad \text{- (1)}$$

$$Q_A = \bar{y}(zA + \bar{z}) + z\bar{A}\overline{(x + y + xy)} \quad \text{- (2)}$$

iii) Obtain the truth table for the next state of the PQ FF.

Hint : You may consider following headings in your truth table

x	y	z	A_n	P_A	Q_A	A_{n+1}

[5 Marks]

Q5 a) i) State the basic function of a flip-flop in a sequential circuit?

ii) If there are *m* different states each with *n* bits, how many flip-flops do you need to implement the memory of the sequential circuit?

iii) Give the logic diagram of a SR flip flop using only NOR gates.

iv) State the characteristic table of the above SR flip- flop.

v) Draw a gated SR Flip Flop with the same characteristic table using NAND gates for the SR Latch.

[5 Marks]

b) i) Draw a logic diagram to illustrate how the gated SR flip flop is modified to form the J K flip flop.

ii) Fill the detailed truth table given in Table Q5 (b) considering the logic diagram drawn in part b) (i). Hence, obtain the characteristic table of the JK flip flop.

iii) For a JK Flip Flop in Master Slave configuration, draw the output waveforms of Master Flip Flop and Slave Flip Flop separately for the given clock signal and J-K inputs as shown in Figure Q5 b). Assume both outputs were 0 prior to the first clock pulse.

Use Figure Q5 b) for your answer and attach it to your answer script.

[5 Marks]

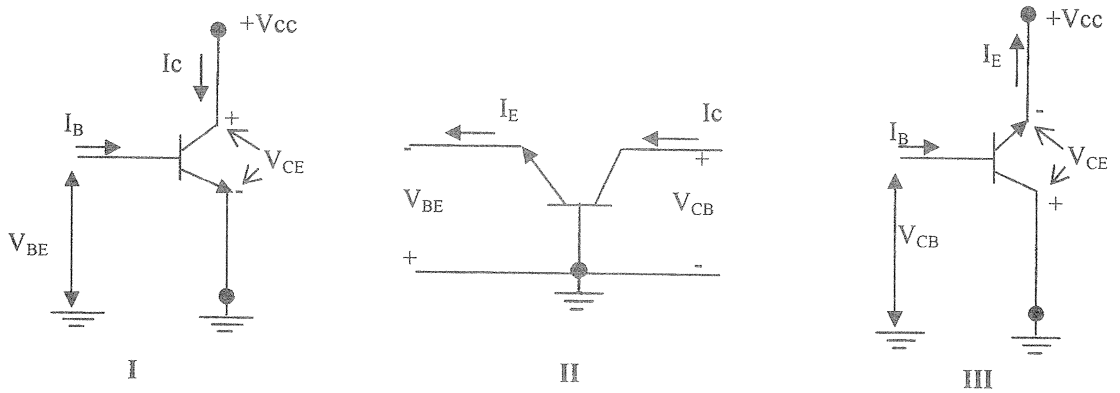

Figure Q1 a)

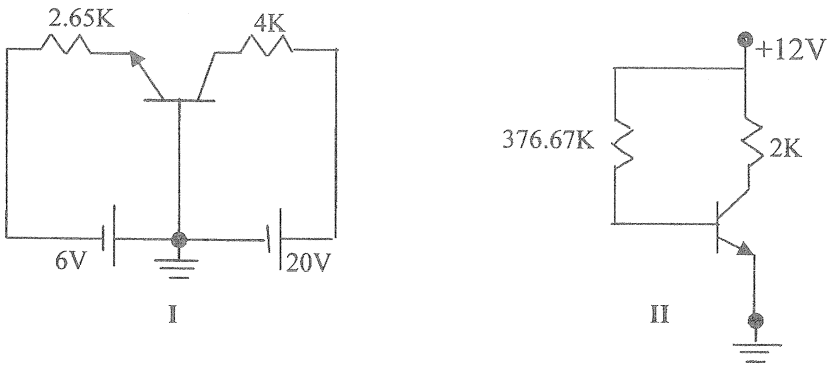

Figure Q1 c)

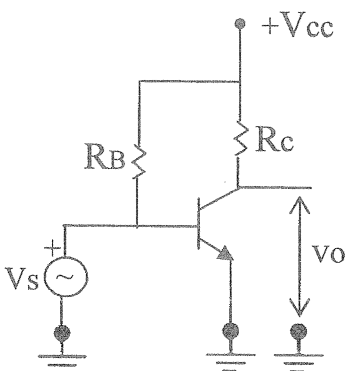

Figure Q2 b)

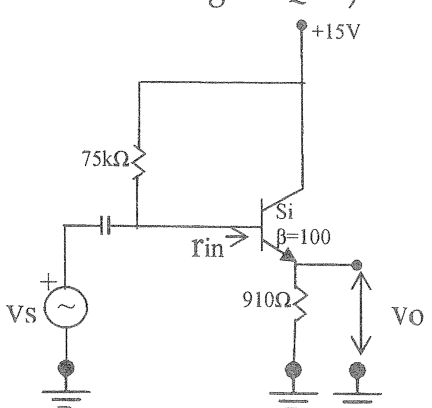

Figure Q2 d)

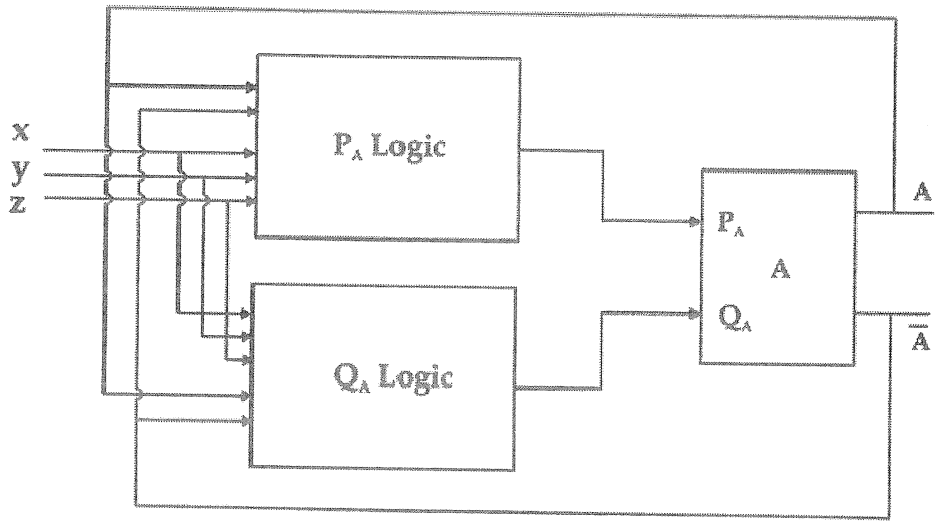

Figure Q4

Table Q5 (b): The detailed truth table for a JK flip-flop

	J_n	K_n	Q_n	$\overline{Q_n}$	S_n	R_n	Q_{n+1}
1	0	0	0	1			
2	0	0	1	0			
3	0	1	0	1			
4	0	1	1	0			
5	1	0	0	1			
6	1	0	1	0			
7	1	1	0	1			
8	1	1	1	0			

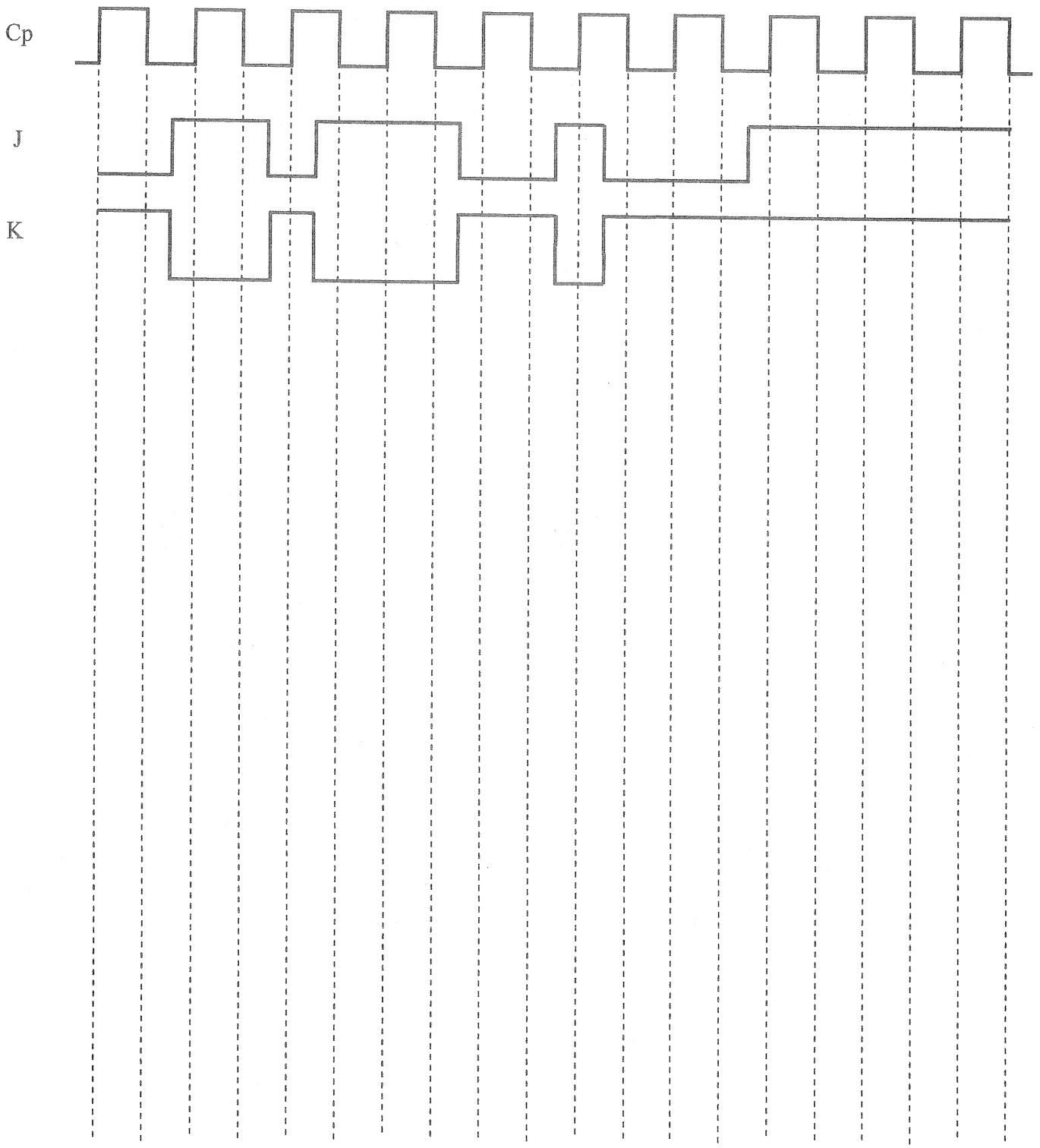

Figure Q5 b)