# UNIVERSITY OF RUHUNA

## Faculty of Engineering

End-Semester 4 Examination in Engineering: December 2016

**Module Number: EE4302** **Module Name: Digital Electronics**

**[Three Hours]**

**[Answer all questions, each question carries 12.5 marks]**

---

Q1 a) i) Draw the block diagram of a sequential circuit and name all the blocks.
ii) What is a state of a sequential circuit?
iii) If there are $m$ different states each with $n$ bits, write an expression to show the relationship between $m$ and $n$.
iv) Briefly explain the equivalent states.

[5.0 Marks]

b) The variation of the output of a special clocked Master slave MN flip-flop (FF) to the variation of inputs M and N is illustrated in Figure Q1(b). Derive the characteristic table and the excitation table of the MN FF.

[1.5 Marks]

c) You are required to design a digital circuit using the state table given in Table Q1(c) with the MN FFs mentioned in Q1 (b).
i) Use the implication table method to reduce the state table.
ii) Make a state assignment to the reduced state table using the binary counting order starting from integer 1.
iii) Draw complete K'maps for the input functions of **only** the first FF and the output.

*Directions : If you have not answered the Q1(b), you may use JK FFs in your design. But you should note that then you will score only half of the marks allocated for the excitation table in the design.*

[4.0 Marks]

d) Construct a **Mealy state diagram** that will detect a serial input sequence of 10010. The detection of the required bit pattern can occur in a longer data string and the correct pattern can overlap with another pattern. When the input pattern has been detected, cause an output z to be asserted high.

[2.0 Marks]

Q2 a) i) Draw a block diagram of an asynchronous sequential circuit (ASC) and indicate the analogy between asynchronous and synchronous sequential circuits (SSC) in the block diagram.
ii) What is meant by the fundamental mode of operation of an ASC?
iii) State two differences between ASCs and SSCs.
iv) Explain the critical and non-critical race conditions in ASCs.

[5.0 Marks]

b) Consider the transition table given in Table Q2(b) and determine all race conditions and whether they are critical or non-critical.

[1.5 Marks]

c) Consider the primitive flow table given in Table Q2(c).

i) Find all compatible pairs by means of an implication table.

ii) Find the maximal compatibles by means of a merger diagram.

iii) Find a minimal set of compatibles that covers all the states and is closed.

[4.5 Marks]

d) Consider the flow table given in Table Q2(d)

i) Convert the flow table into a transition table by assigning the binary values to the states: *a = 00, b = 01* and *c = 11*, in such a way as to avoid the critical race conditions.

ii) Assign outputs to the don't care states to avoid transient output pulses.

[1.5 Marks]

Q3 a) i) Name three logic families.

ii) What is meant by propagation delay and noise immunity of a logic gate?

iii) Explain the operation of the DTL NAND circuit shown in Figure Q3(a) when both inputs A and B are high (+5 V ≡ logical 1).

[5.0 Marks]

b) The output $V_0$ of the DTL NAND gate shown in Fig. Q3(a) is connected to the N different inputs ($A_1$, $A_2$,.., $A_N$) of other similar N gates. Both the inputs of the source (original) gate (A and B) are kept at high. The given DTL circuit has 2 kΩ, 1.8 kΩ, 5 kΩ and 2 kΩ for R1, $R_2$, $R_3$ and $R_4$ respectively. For both transistors ($T_1$ and $T_2$), $h_{FE} = 20$, $V_{BE} = 0.7$ V and $V_{CE(sat)} = 0.2$ V. All the diodes are silicon and the collector supply ($+V_{CC}$) is 5 V.

i) Calculate the current in the 2 kΩ resistor.

ii) Calculate the current coming from each input connected to the source gate.

iii) Express the total collector current in transistor $T_2$ in terms of N.

iv) Find the base current ($I_B$) of transistor $T_2$.

v) Find the value of N that keeps $T_2$ in saturation. Hence find the fan-out of the gate.

[4.0 Marks]

c) A switching network has two control inputs $C_1$, $C_2$ and one data input D. The output Z for each combination of inputs is decided as follows,

If $C_1$=$C_2$=0 and D=1, the output is $Z = 0$

If $C_1$=$C_2$=1, the output is $Z = 1$

If $C_1$=1 and $C_2$=0, the output is $Z = D$

If $C_1$=0 and $C_2$=1, the output is $Z = \overline{D}$

i) Derive the truth table for Z.

ii) Implement the switching network using minimum number of **only** NAND gates

[3.5 Marks]

Q4 a) i) What are the main steps involved in analog to digital (A/D) conversion?

ii) Sketch the following discrete sequences.

I $U(n-1)$ II $U(n)-U(n-2)$

III $2\delta[n-2]+4\delta[n-3]-\delta[n-4]$ IV $\left(\frac{1}{2}\right)^n U(n)$

[3.5 Marks]

b) Determine the output voltage of the D/A converter shown in Figure Q4(b) when the input is 101.

[1.0 Mark]

c) Consider a discrete LTI system with impulse response $h(n)$, input $x(n)$ and output $y(n)$. Where,

$$x(n)=\begin{cases}5^n & ;n<0\\ 3^n & ;n\geq 0\end{cases} \qquad h(n)=\left(\frac{1}{2}\right)^{|n|}$$

i) Define the Z-transform of a discrete sequence $x(n)$.

ii) What is the relationship between $x(n)$, $y(n)$ and $h(n)$ in the time domain and the Z-domain?

iii) Determine the Z-transform for $x(n)$ and $h(n)$, hence find the region of convergence for both sequences.

iv) Find the output $y(n)$

[6.0 Marks]

d) A discrete system equation is given by

$$y[n]-\sum_{k=1}^{N}a_k y[n-k]=\sum_{k=0}^{M}b_k x[n-k]$$

i) Obtain the impulse response in the Z-domain.

ii) What is the condition for infinite impulse response (IIR) system.

iii) Find the finite impulse response (FIR) system equation.

[2.0 Marks]

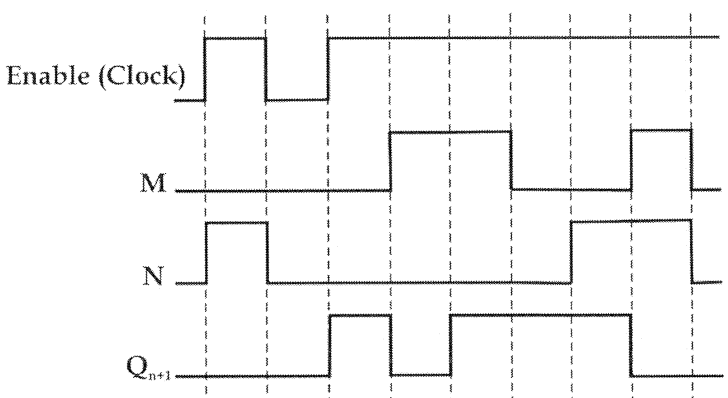


Figure Q1(b)

Table Q2(c) : State Table

| Present state | Next state | | Output | |
|---|---|---|---|---|
| | X=0 | X=1 | X=0 | X=1 |
| a | f | b | 0 | 0 |
| b | d | c | 0 | 0 |
| c | f | e | 0 | 0 |
| d | g | a | 1 | 0 |
| e | d | c | 0 | 0 |
| f | f | b | 1 | 1 |
| g | g | a | 0 | 1 |

Table Q2(b) : Transition Table.

| $y_1y_2$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 10 | 10 | 11 | 00 |
| 01 | 01 | 10 | 10 | 00 |
| 11 | 01 | 11 | 11 | 00 |
| 10 | 11 | 10 | 10 | 00 |

Table Q2(c) : Primitive Flow Table.

| $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| a | a, 0 | b, – | –, – | e, – |
| b | a, 0 | b, 0 | a, – | –, – |
| c | –, – | d, – | c, 0 | e, – |
| d | a, – | d, 1 | –, – | –, – |
| e | a, – | –, – | b, – | e, 0 |
| f | –, – | b, – | f, 0 | e, – |

Table Q2(d) : Flow Table

| $y_1y_2$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| a | a, 0 | b,– | c, – | a, 1 |
| b | a, – | b, 0 | b, 1 | c, – |
| c | a, – | c, 1 | c, 0 | c, 1 |

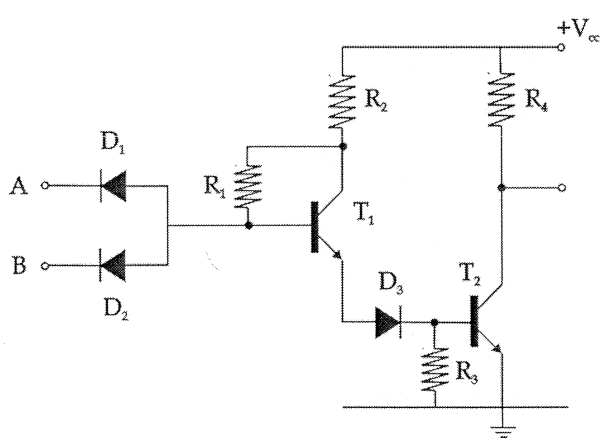


Figure Q3(a): DTL NAND Circuit

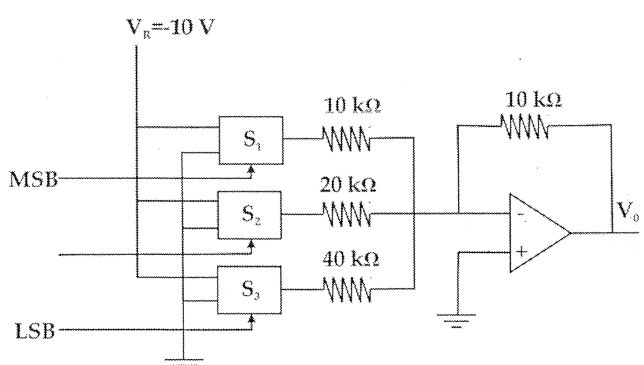


Figure Q4(b): Summing D/A converter Circuit