UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 2 Examination in Engineering: December 2015

Module Number: EE2202 **Module Name: Introduction to Electronic Engineering**

[Three Hours]

[Answer **all questions**, each question carry ten marks]

Q1 Short answer questions.

[Questions 1 to 17 carries 0.5 marks each and question 18 carries 1.5 marks]

1) State the difference between an analog and a digital signal.
2) State what is meant by the frequency spectrum of an analog signal.
3) Give the powers of 10 for the abbreviations Giga (G), Mega (M), kilo(k), Mili (m), Micro (μ) and Nano (n).
4) State the number of valence electrons in a Silicon (Si) atom.
5) State the number of valence electrons in Group 13 and Group 15 elements in the Standard Periodic Table.
6) Describe what is meant by a covalent bond.
7) State how a PN junction diode is formed.
8) Give the polarity of a DC supply to forward bias and reverse bias a diode.
9) When a DC supply is connected to the diode, define the charge carriers that contribute to the current flow in
   i) the semiconductor
   ii) the external circuit
10) Define the regulating region of a Zener diode.
11) In an elementary DC power supply, state the functions of
   i) the rectifier
   ii) the capacitor
12) Convert 74_{10} to binary
13) Convert $1010\ 0101_2$ to decimal
14) Draw the circuit symbol for a two input NAND gate and give its Boolean equation and the truth table.
15) Draw the circuit symbol for a two input NOR gate and give its Boolean equation and the truth table.
16) Add $8_{10} + 3_{10}$ using binary arithmetic.
17) Prove the Boolean expression $A + 1 = 1$
18) Use the Karnaugh map reduction technique to simplify the Boolean expression

$$X = \left(\overline{A}\,\overline{B} + A\,\overline{B}\right)\overline{C} + C\left(AB + A\overline{B}\right)$$

and draw the combinational logic circuit to implement the result.

Q2 a) Figure Q2 a) shows a Si transistor bias circuit.

i) Define the configuration shown in Figure Q2 a).

ii) Reproduce the typical output characteristics for this configuration.

iii) Give the load line for the circuit.

iv) Determine the operating point of the transistor assuming the Emitter-Base junction is forward biased and taking a reasonable value for the current gain α for a good transistor.

[3 Marks]

b) Figure Q2 b) shows the circuit for calculating the leakage current of a transistor.

i) Define the configuration shown in Figure Q2 b).

ii) Define the notation I_{CEO} for the leakage current given that $I_c = \alpha I_E + I_{CBO}$ with the usual notations.

iii) Formulate an expression relating the input and output currents.

iv) Define the current gain β for $I_{CEO} = 0$.

v) Express the current gain α in a) in terms of β.

[3.5 Marks]

c) Figure Q2 c) shows the bias circuit for a Si transistor.

i) Define the configuration shown in Figure Q2 c).

ii) Formulate an expression for I_B given that $I_E = (\beta+1) I_B$.

iii) Determine the bias point of the transistor for $R_B = 115\ k\Omega$, $R_E = 1\ k\Omega$, $Vcc = 16\ V$ and $\beta = 120$.

[3.5 Marks]

Q3 a) i) Explain the purpose of biasing an amplifier and the effect of incorrect bias.

ii) Describe amplitude distortion with reference to bias in an amplifier.

[2.5 Marks]

b) i) Figure Q3 b) i) shows the AC equivalent circuit for a Si transistor in Common-Base configuration. Using the same notation, define the input resistance and generate the AC equivalent circuit for the Si transistor in Common-Emitter configuration. The output resistance is given by r_c/β. Notations have their usual meanings.

ii) Figure Q3 b) ii) shows a Common-Emitter amplifier. By carrying out the AC analysis, formulate expressions for the voltage gain A_v and the current gain A_i of the amplifier.

iii) If a load resistance R_L is connected to the amplifier in part ii)

I. Redraw the AC circuit and write an expression for the overall voltage gain.

II. Considering the load resistance terms only, explain the effect of AC load resistance on overall voltage gain.

[4.5 Marks]

c) i) Reproduce the typical output characteristics and identify the regions for a NPN Si transistor to be operated as a switch.

ii) Give the circuit of a NPN Si transistor as a switch and briefly explain its operation for an input square pulse waveform.

[3.0 Marks]

Q4 a) i) Sketch the structure of an N-type Junction Field Effect Transistor (JFET) and denote the terminals.

ii) Draw the circuit symbols for N-type and P-type JFETs.

iii) Describe with the aid of diagrams, the two ways depletion regions are generated in an N-type JFET.

iv) Describe the pinch-off condition.

v) Sketch the drain and transfer Characteristics for an N- type JFET and identify the different regions of operation.

[5 Marks]

b) i) Define the acronym MOSFET.

ii) Give the circuit symbols for an N-type depletion type MOSFET and an enhancement type MOSFET.

iii) Show the structure and the bias for an N-type depletion type MOSFET.

iv) Show the structure and the bias for a P-type depletion type MOSFET.

v) State how the N-type depletion MOSFET can be used in the enhancement mode of operation.

vi) Sketch the typical drain characteristics for this MOSFET operating in the depletion and enhancement modes.

[5 Marks]

Q5 Use the provided sheet of Figure Q5 for your answers and attach it to your answer script.

a) i) Give the circuit of a cross-NOR SR flip flop, its circuit symbol and its function table.

ii) Give an alternate circuit that has the same function table as part i).

iii) Modify the circuit in part i) to give a Gated SR flip flop and give its function table.

iv) Figure Q5 a) gives the Gate (enable) and the S and R inputs for a Gated SR flip flop. Synthesize the output Q and indicate the Set, Reset and Hold conditions.

v) Give the circuit for a J-K flip flop and its function table.

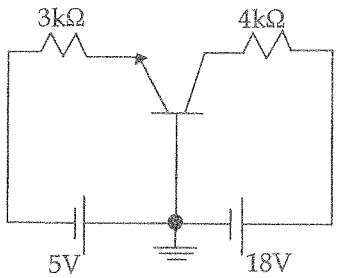
[5 Marks]

b) i) Explain what is meant by and the advantages of positive edge and negative edge triggering.

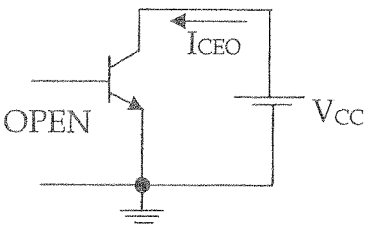
ii) State the meaning of a MOD-8 binary counter and list the counting sequence.

iii) Give the circuit for a MOD-8 ripple counter with negative edge triggered J-K flip flops and synthesize its output waveforms and the counting sequence in Figure Q5 b).

[5 Marks]



a)



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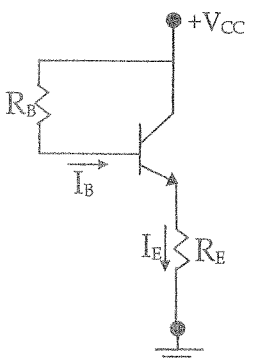
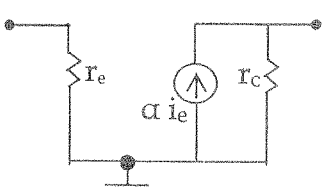
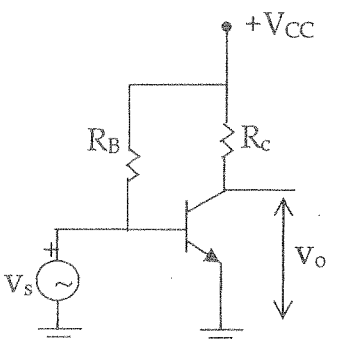


c)

Figure Q2



i)



ii)

Figure Q3 b)

Index No:

Q5 Answer sheet. Attach this to you main answer script.

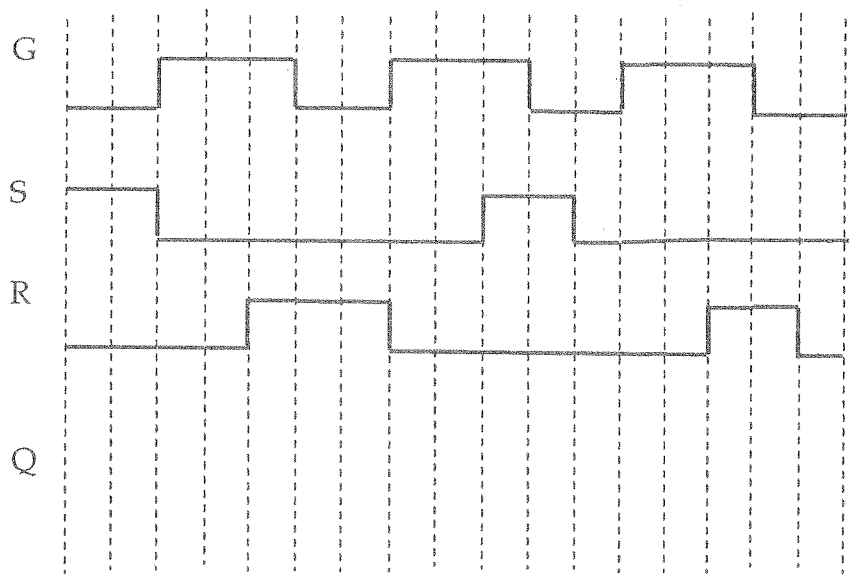


Figure Q5 a)

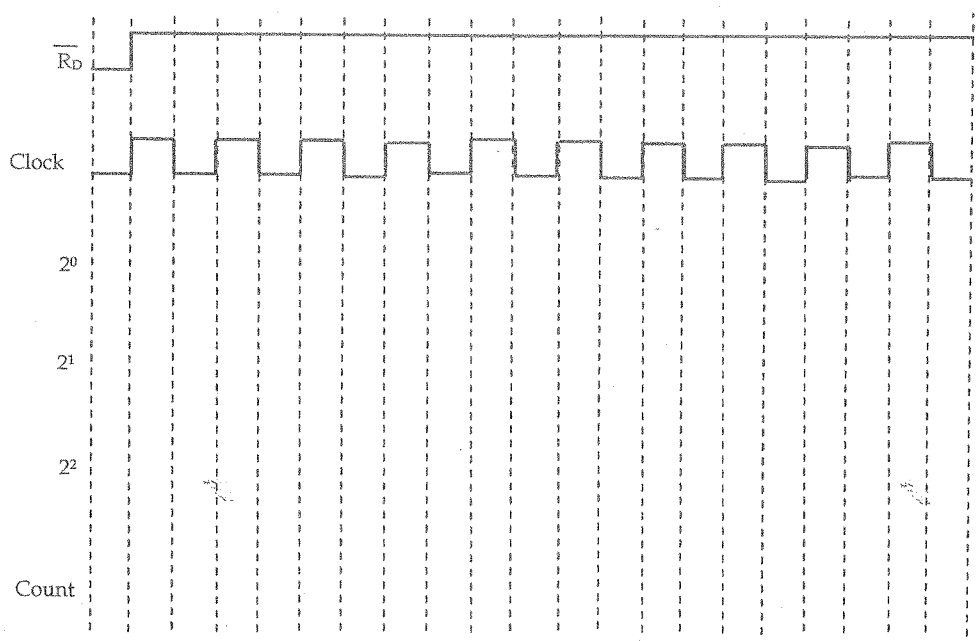


Figure Q5 b)