UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 2 Examination in Engineering: July 2022

Module Number: EE2202 Module Name: Introduction to Electronic Engineering

[Three Hours]

[Answer **all questions**, each question carries **10** marks]

Q1 a) i) Briefly explain the concept of diffusion and drift of charge carriers in semiconductors.

ii) Briefly explain how the PN junction behaves under the equilibrium state.

[3.0 Marks]

b) Figure Q1.1 shows a Si diode circuit used to add a dc level to a signal with an average value of zero. v_S is a square wave alternate between 10 V and -10 V. The period of the square wave is T.

i) Plot the output (v_L) over time (t) considering the constant voltage model for the diode.

ii) Find the average value of the output signal.

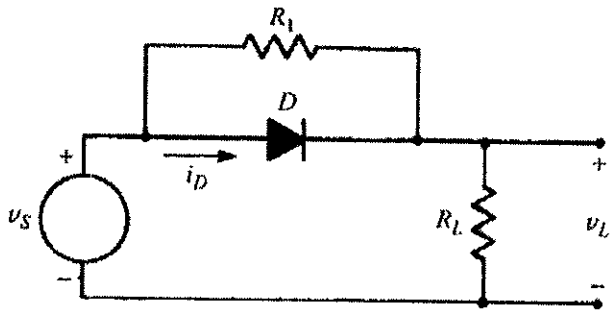

Figure Q1.1

[4.0 Marks]

c) Figure Q1.2 shows the function ReLU (Rectified Linear Unit), which is used as an activation function in artificial neural networks. Propose a diode circuit to perform the ReLU function to a given input voltage, assuming that the diode is ideal.

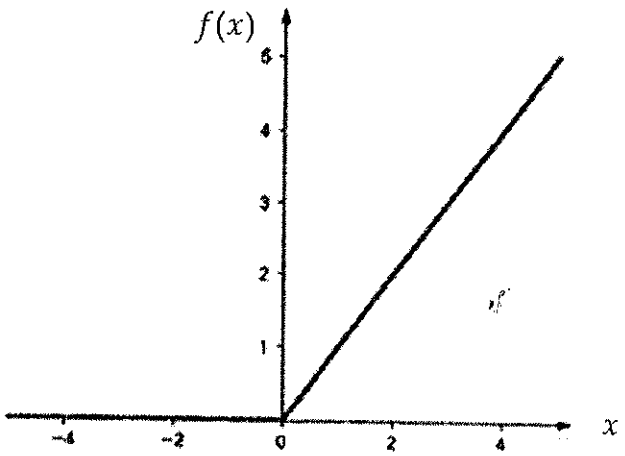

Figure Q1.2

[3.0 Marks]

Q2 a) i) State the three main regions of a BJT transistor and sort them based on doping levels.

ii) State the rule for biasing along with the bias circuit with no external resistors and current equation for an *NPN* Si transistor in Common-Base configuration.

iii) Sketch the output characteristics for a *NPN* Si transistor in common based configuration and saturation, active and cut-off regions.

[6.0 Marks]

b) Figure Q2 shows biased circuit with resisters for a *NPN* Si transistor in common based configuration.

i) Derive an expression for the load line.

ii) Find R_C and R_E of the circuit when V_{CB} = 4 V, I_C = 3 mA, V_{BE} = 0.7 V, $V_{CC} = -V_{EE}$ = 10 V and β = 120.

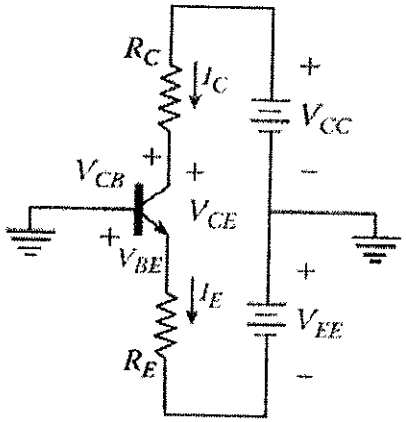

Figure Q2

[4.0 Marks]

Q3 a) Figure Q3.1 shows the schematic diagram of a transistor amplifier with the source and load.

i) Derive an expression for the overall voltage gain (v_L / v_S), where the voltage gain of the amplifier is A_v.

ii) Based on the derived expression in part i), identify suitable input resistance (high or low) for a voltage amplifier.

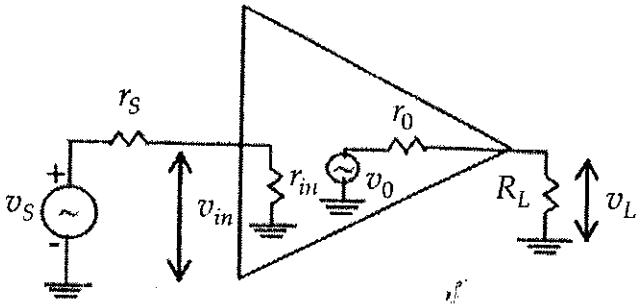

Figure Q3.1

[3.0 Marks]

b) Figure Q3.2 shows a CE amplifier in its simplest configuration.

i) Briefly explain the role of C_{B1} and C_{B2} capacitors in the amplifier circuit.

ii) Find the R_1 and R_C to fix the Q-point at I_{CQ} = 30 mA and V_{CEQ} = 10 V (V_{CC} = 20 V, β = 50).

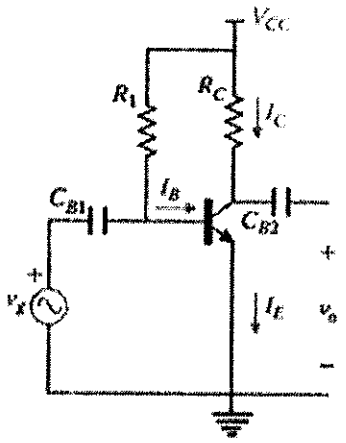

Figure Q3.2

[4.0 Marks]

c) Sketch the internal structure of an *N*-type Enhancement MOSFET, name the terminals and briefly explain the mechanism behind the formation of the *N*-channel in a biased E-MOSFET.

[3.0 Marks]

Q4 a) Obtain the 1's and 2's complements of the following binary numbers.

i) 11011010

ii) 10000101

[3.0 Marks]

b) Convert the following expressions to Product-of-Sums (PoS) form.

i) $Z = A + \bar{B}CD$

ii) $W = \bar{C}D + \bar{C}\bar{E} + \bar{G}H$

[3.0 Marks]

c) Reconstruct the logic circuit shown in Figure Q4 using only NOR gates.

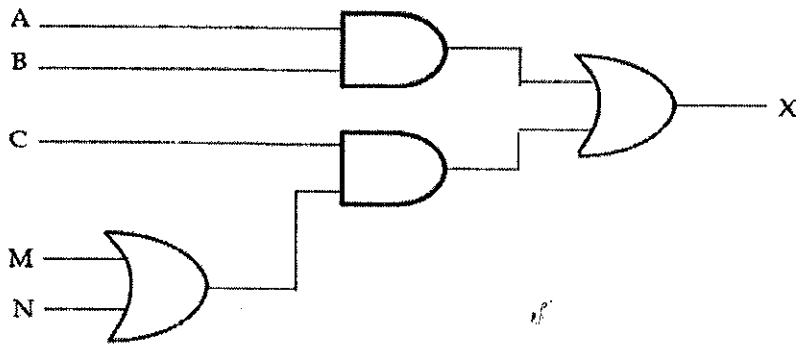

Figure Q4

[4.0 Marks]

Q5 a) Briefly explain the difference between combinational and sequential logic circuits using illustrations.

[2.0 Marks]

b) Simplify the following Boolean function F, together with don't care terms in d, using a four-variable Karnaugh map.

$$F\,(A, B, C, D) = \sum(2, 4, 6, 10, 12)$$
$$d\,(A, B, C, D) = \sum(0, 8, 9, 13)$$

[4.0 Marks]

c) Obtain the characteristic table for the clocked SR Flip-Flop shown in Figure Q5.

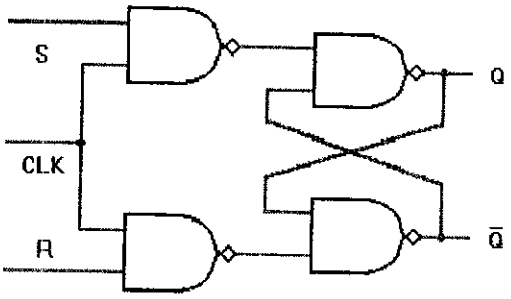

Figure Q5

[4.0 Marks]