

**University of Ruhuna - Faculty of Technology**  
**Bachelor of Information Communication Technology Honours Degree**  
**Level 1 (Semester II) Examination - November/December 2025**  
**Academic Year 2024/2025**

Course Unit: **ICT1252 – Computer Architecture**

Duration: 2 hours

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This question paper contains 03 pages, including this instruction page.

**IMPORTANT INSTRUCTIONS:**

1. The medium of this examination is English.
2. Answer all four (04) questions.

**Question 01**

a)

- i. Briefly explain how Harvard architecture overcomes the drawbacks of Von Neumann architecture. (15 marks)
- ii. List and briefly explain the main structural components of the CPU. (15 marks)
- iii. Write down four (04) slots/sockets contained in a computer motherboard. (10 marks)
- iv. Describe the four (04) main steps of the instruction cycle relevant to CPU. (10 marks)

b)

- i. Name five (05) types of processor registers and describe four (4) of them (30 marks)
- ii. Briefly explain what is an operation code (opcode) using an example of an instruction code in a hypothetical machine. (20 marks)

### Question 02

- a)
- Why does a computer system require interrupts? Explain your answer with a suitable example. (15 marks)
  - Briefly explain two (02) advantages and one (01) disadvantage of using interrupts in computer systems. (15 marks)
- b)
- What is a Computer Bus? (10 marks)
  - Explain the three (03) main types of system bus lines and their functions. (15 marks)
  - What is bus arbitration, and what are the two (02) main types of bus arbitration used when multiple devices request control of the bus simultaneously? (15 marks)
- c) Briefly explain the following terms with respect to magnetic disks. (30 marks)
- Sector
  - Intertrack gap
  - Constant Angular Velocity (CAV)

### Question 03

- a)
- Calculate the check bits for the data word 1101 using the **Hamming error correction code**. Fill the position number, data bits, and control bits according to the following table. (20 marks)

| Bit position    | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|-----------------|---|---|---|---|---|---|---|
| Position number |   |   |   |   |   |   |   |
| Data bits       |   |   |   |   |   |   |   |
| Control bits    |   |   |   |   |   |   |   |

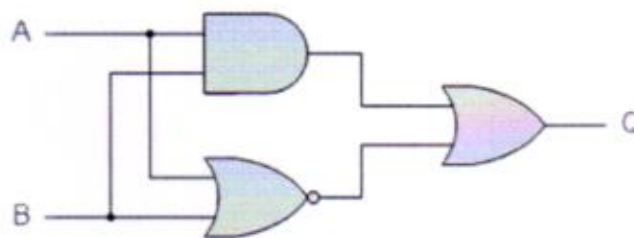
- Illustrate the above data bits and control bits in a Venn diagram. (10 marks)
- b)
- Solve the following two calculations using 8-bit 2's complement notation. (25 marks)
- $17+19$
  - $17-19$

- c)
- i. Explain the key features of a multiprogramming operating system. (15 marks)
  - ii. Briefly explain the “Swapping” in memory management. (15 marks)
  - iii. What is the main purpose of using RAID in external storage devices? (15 marks)

**Question 04**

- a)
- i. Briefly explain the direct and sequential access of computer memory. (10 marks)
  - ii. Explain the concept of cache memory and describe how temporal and spatial locality improve its performance. (25 marks)
- b)
- i. Briefly explain the associative mapping technique used in cache memory. (15 marks)
  - ii. A system uses a direct-mapped cache of 8 KB with a block size of 64 bytes. Determine the number of lines in the cache. (10 marks)
- c)
- i. Simplify the following Boolean expression using Boolean algebra laws and rules. Show each step clearly and indicate which law or rule is applied at every step. (20 marks)  

$$M = AB + A(B + C) + B(B + C)$$
  - ii. Draw the truth table and write the Boolean expression for the following logic circuit. (20 marks)



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