University of Ruhuna- Faculty of Technology

Bachelor of Engineering Technology Honours Degree
Level 2 (Semester II) Examination, November/December 2025
Academic year 2023/2024

Course Unit: ENT 2213- Digital Electronic Systems (Written) **Duration: 03 hours**

- All symbols have their usual meanings.
- This paper contains **five (05)** questions on **five (05)** pages.
- All questions carry equal marks.
- Answer **all** the questions.
- Please mention all the assumptions, if any.

1)

a.

i. List two (02) advantages of using a digital thermometer instead of an analog thermometer for industrial temperature measurements. (2 marks)

ii. Briefly explain how to implement NOT gate function using an XOR gate. (2 marks)

b.

i. State De Morgen's theorems. (2 marks)

ii. Draw the equivalent logic circuits to demonstrate De Morgen's theorems. (2 marks)

iii. Reduce the Boolean expression, $Y = \overline{\overline{P}\overline{Q}}.\overline{R}$ using the De Morgen's theorems. (2 marks)

c. An autonomous delivery drone carries a small package. Base on a binary select input, it should automatically decide to drop the package on one of four drop-off zones (Zone A, Zone B, Zone C and Zone D).

i. What is the minimum number of bits required for the select input? (1 mark)

ii. Define the inputs and four (04) outputs of a suitable digital system for above purpose and draw the corresponding truth table. (2 marks)

iii. Draw the logic circuit implementation corresponding to the truth table drawn in part ii) using discrete logic gates. (3 marks)

iv. Identify a method to implement the same digital system without using discrete logic gate ICs. (1 mark)

v. Using the circuit symbol of the digital device corresponding to the method identified in part iv), draw the logic circuit implementation of the same system without using discrete logic gate ICs. (3 marks)

2)

a.

i. Name two (02) disadvantages of using Boolean algebra to minimize Boolean expressions. (2 marks)

ii. Given that all four inputs will not be logic high at the same time in the digital system represented by the Boolean expression $Y = A\bar{B}C\bar{D} + A\bar{B}CD + ABC\bar{D}$, using a suitable method, find the minimized version of the Boolean expression resulting in the least number of gates possible. (3 marks)

b.

i. Name two (02) applications of binary encoders. (2 marks)

ii. Draw the truth table of the decimal to BCD (Binary Coded Decimal) encoder. (2 marks)

iii. Draw the logic circuit of the decimal to BCD encoder corresponding to the truth table drawn in part ii). (2 marks)

c. It is required to design an active high logic digital system to identify numbers divisible by four (04) excluding zero from input of 4-bit binary numbers.

i. Define suitable inputs and output of a suitable digital system for above purpose and draw the truth table for the output. (2 marks)

ii. Find the minimized SoP (Sum of Products) Boolean expression for the output using Karnaugh map(K-map). (3 marks)

iii. Suggest a method to implement above minimized Boolean expression without using discrete gate ICs. (1 mark)

iv. Using the circuit symbol of the digital device corresponding to the method identified in part iii), draw the logic circuit implementation of the minimized Boolean expression without using discrete logic gate ICs. (3 marks)

3)

a. The control unit of a smart EV (Electric Vehicle) home charger receives a master oscillator at 100 kHz. The low frequency battery-protection subsystem operates at 6.25 kHz.

i. Name the property of flip flop circuits that can be used to obtain 6.25 kHz. (1 mark)

ii. Draw the suitable logic circuit to obtain 6.25 kHz. (No need to draw the gate level implementation, use the circuit symbols) (2 marks)

b.

i. Draw the circuit symbol of a negative edge triggered JK flip flop. (2 marks)

ii. Separately draw the modification required to form a T flip flop using a negative edge triggered JK flip flop. (2 marks)

iii. Classify two (02) main types of counters based on feeding clock signal. (2 marks)

iv. How many flip flops are required to implement a digital counter to count from 0 to 255. (2 marks)

c. A seminar room has a maximum capacity of fifteen (15) seats. It is required to turn on an LED to indicate that the room is fully occupied when fifteen people enter the room. There is a sensor that generates a square pulse when a person enters the room.

i. Identify the digital counter required for above purpose. (1 mark)

ii. Draw the compete circuit diagram of a suitable digital system using the circuit symbol of a suitable flip flop. (6 marks)

iii. Name one drawback of the digital system drawn in part ii). (2 marks)

4)

a.

i. Draw the logic circuit of a level triggered JK latch. (2 marks)

ii. Identify the major drawback of the circuit drawn in part i). (1 mark)

iii. Separately draw a modified version of the logic circuit drawn in part i) to avoid the drawback identified in part ii). (2 marks)

b.

i. Name two (02) types of shift registers. (2 marks)

ii. Draw the circuit diagram of a shift register required to obtain 3-bit input serial data simultaneously in the output. (2 marks)

iii. Draw the timing diagrams for the outputs of the flip flops in the shift register drawn in part ii) corresponding to an input bit sequence of 101. Use the Annexure I and attach it to the end of the answer script. (5 marks)

c.

i. Identify the type of shift register required to introduce a constant delay in a digital circuit. (1 mark)

ii. Briefly explain how the shift register identified in part i) can be used to introduce a constant delay in a digital circuit. (3 marks)

iii. Calculate the time delay introduced by a 32-bit shift register of the type identified in part ii) when operated with a 4 MHz clock. (2 marks)

5)

a.

i. Name two (02) factors to consider when selecting an analog to digital converter. (2 marks)

ii. Identify two (02) methods to increase the accuracy of an analog to digital converter. (2 marks)

iii. Briefly explain one of the methods identified in part ii). (2 marks)

b. A 10-bit analog to digital converter gives a digital output of 0110101010 for an input of 5 V.

i. What is the smallest voltage that can be converted with this analog to digital converter. (3 marks)

ii. What is the largest voltage that can be converted with this analog to digital converter. (3 marks)

c.

i. Name one disadvantage of Binary Weighted Resistor type digital to analog converter. (1 mark)

ii. Draw the circuit diagram of a 3-bit Binary Weighted Resistor type digital to analog converter. (3 marks)

iii. Calculate the output voltage of the digital to analog converter drawn in part ii) corresponding to a digital input of 101. Take $V_{ref} = 12V$ and $2R_f = R$ under usual notation where V_{ref} and R_f are reference voltage and feedback resistor respectively. (4 marks)

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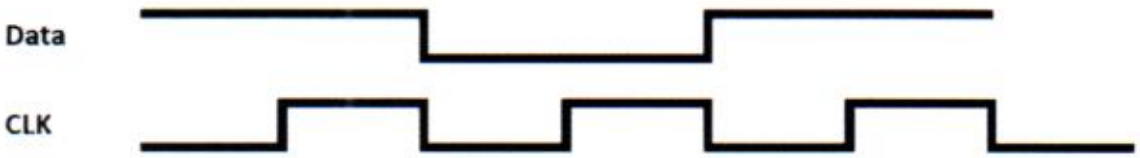
Annexure I

4) b) iii)



Q0 (LSB)

Q1

Q2 (MSB)