UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 8 Examination in Engineering: January 2026

Module Number: EC8207 Module Name: IC Design (TE) (C-18)

[Three Hours]

[Answer all questions, each question carries 12.5 marks]

Q1 a) Write key main steps in digital IC design flow and briefly explain each step.

[3.5 marks]

b) Synthesis is an important step in the design flow.

i) What is synthesis and explain the key steps involved?

[1.5 marks]

ii) Name two logic optimization techniques and key differences in the identified techniques.

[1.0 mark]

iii) What is the difference between logic synthesis and layout synthesis?

[1.0 mark]

c) Estimate minimum die size as per the information given below. All dimensions are given in micrometers. Assume 90% utilization margin can be reached since this is a small design.

- IO pad - qty = 21 , W = 20 , H = 60
- Power pad - qty = 2 each side of the die , W = 30 , H = 60
- Filler pad - qty = as required , W = 10 , H = 60
- Corner cells - W = 60 , H = 60
- SRAM - W = 60 , H = 200
- Logic cell type A - qty = 30 , W = 4 , H = 5
- Logic cell type B - qty = 20 , W = 8 , H = 5
- Logic cell type C - qty = 10 , W = 12 , H = 5
- Logic cell type D - qty = 15 , W = 16 , H = 5

[5.5 marks]

Q2 a) What is the difference between RTL simulation and Gate Level simulation?

[2.0 marks]

b) Explain two significant hadships in RTL Simulation.

[2.0 marks]

c) What are the three classifications into which FPGAs can be divided based on their internal block arrangement? Explain each of the them.

[3.0 marks]

d) By using the Formal Verification concepts, answer the following questions.

i) What are the partitions we can generate to prove the equivalence of the circuits given in Figure Q2(d-1) and Figure Q2(d-2).

[1.0 mark]

ii) Prove two circuits given in Figure Q2(d-1) and Figure Q2(d-2) named as Circuit Diagram 1 and Circuit Diagram 2, respectively, are equivalent. You may use Boolean algebra or Truth-tables.

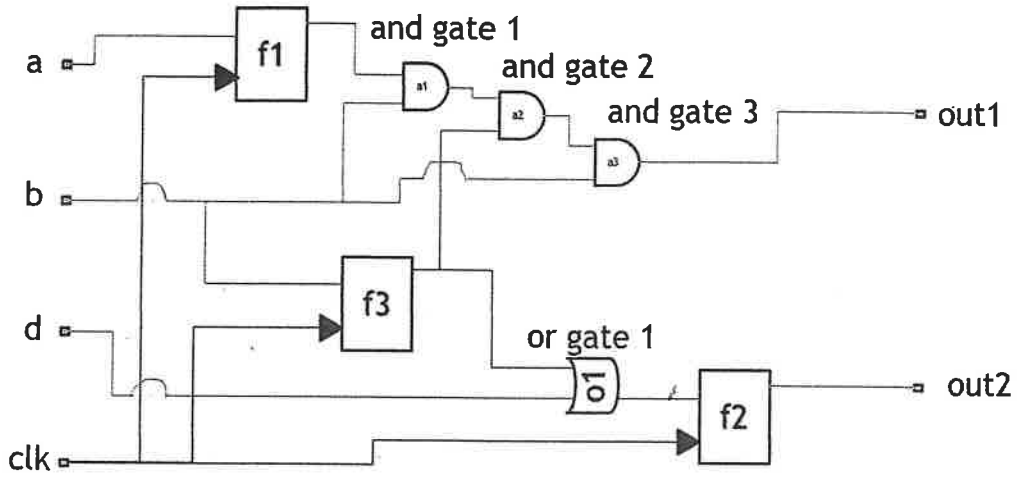

Figure Q2(d-1) Circuit Diagram 1

Note for the circuit diagram 1:
d drives only **o1** (or gate 1)
b only drives **f3**, **a1** and **a3**

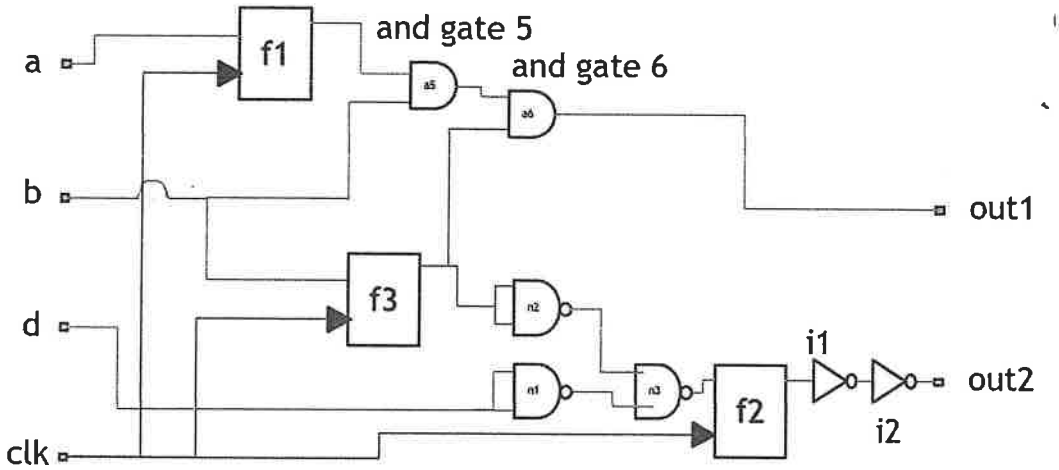

Figure Q2(d-2) Circuit Diagram 2

Note for the circuit diagram 2:
d drives only **n1**
b only drives **f3** and **a5**

[4.5 marks]

Q3 a) Clearly name 3 Verilog/ System Verilog syntaxes which used to
a. Indicate the end of a simulation.
b. Print messages or values to the simulation console.
c. Continuously check/ display changes to specified variables on the console.

[1.5 marks]

b) Assume you have 3 variables, named Var1, Var2 and Var3. Using the appropriate syntax, write the Verilog/ System Verilog code to continuously check/ display changes of those variables on the console. Expected console output format is given below.
Variable value change detected. New values are Var1 = 11 Var2 = 10 Var3 = 111

[1.5 marks]

c) Briefly explain the meaning/functionality of following Verilog lines.

I. assign Out = (A == 4'b1111) ? B : 1'b0;

II. B <= 8'b00000001 << A;

[2.0 marks]

d) Find and briefly explain the errors/ bad practices in following Verilog module/ testbench snippets and rewrite the corrected versions.

a)

```
module test(
   input wire [2:0] select,
   output reg out
);
always @( select) begin
   case (select)
      2'b000: out = 1'b0;
      2'b101: out = 1'b1;
      2'b010: out = 1'b0;
      2'b011: out = 1'b1;
   endcase
end
endmodule
```

b)

```
module testbench( );
   reg CLOCK;
   dummy_module dut (
      .CLOCK(CLOCK)
   );
   initial begin
      forever #1 CLOCK =
~CLOCK;
   end
endmodule
```

[2.0 marks]

e) Write Verilog module called "Dff" to follow the logical operation of a generic D flip flop. Use the "Dff" module to write Verilog module called "Div4" which divides the input clock frequency by 4 (eg. Cout frequency is 10Hz when Cin frequency is 40Hz). Follow the names on the diagrams.

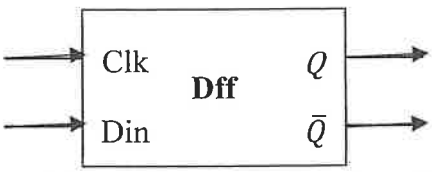

Figure Q1(e-1) Dff module diagram

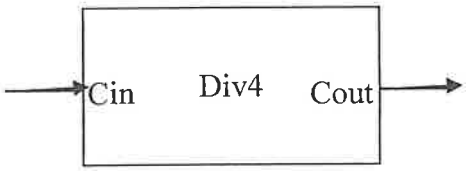

Figure Q3(e2) Div4 module diagram

[2.5 marks]

f) Write the Verilog module called "CD4017" to imitate the logical functionality of CD4017 decade counter with 10 outputs using behavioral modeling. Input/output names of the module and timing diagram are given below. Follow the names on the diagrams.

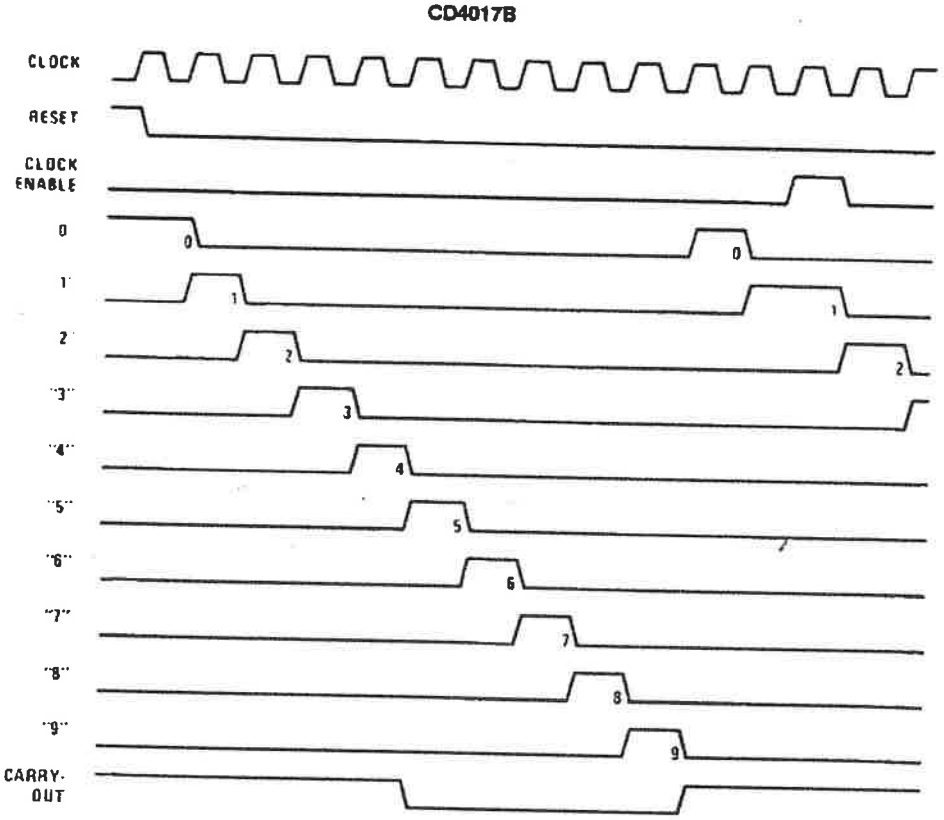

Figure Q3(f-1) Timing diagram of the decade counter

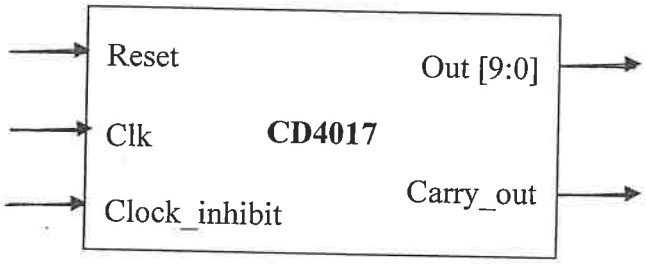

Figure Q3(f-2) Diagram of the decade counter

[3.0 marks]

Q4 a) This is a 3D view of a high-speed PCB transmission line in microstrip configuration. To answer the below (b) and (c) questions, you may use a cross-sectional view of the transmission for this.

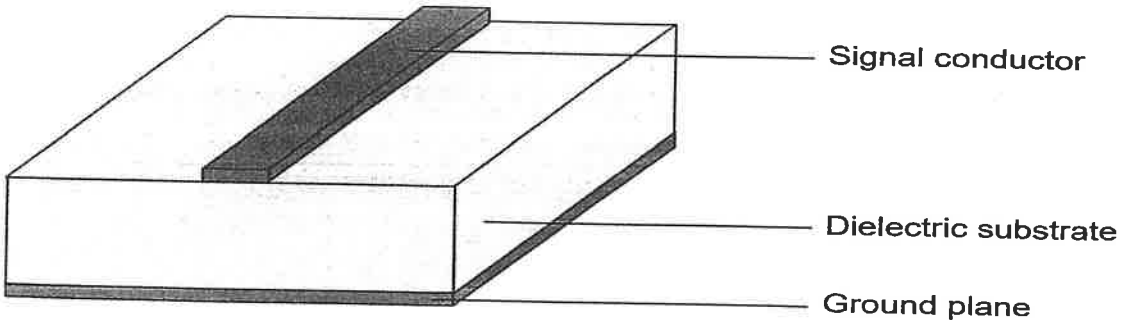

Figure Q4(a) Diagram of the High-speed PCB line

i) Where does the majority of the signal's energy flow?

[3.5 marks]

ii) Draw the electric field of the transmission line

[2.0 marks]

iii) Draw the magnetic field of the transmission line.

[2.0 marks]

b) Below image shows a few copper traces/tracks of a PCB layout. It has two regions marked as A and B.

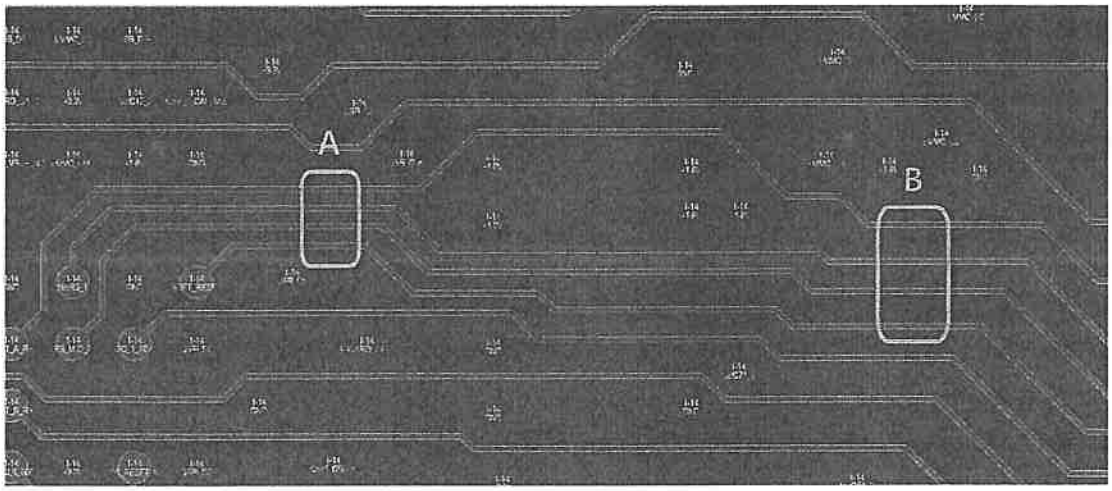

Figure Q4(b) Diagram of copper traces and tracks of the PCB Layout

i) Which region has the minimum crosstalk.

[1.5 marks]

ii) Explain the reason for your answer in (i)

[3.5 marks]