# UNIVERSITY OF RUHUNA

**Faculty of Engineering**

End-Semester 3 Examination in Engineering: March 2026 (C-23)

**Module Number: EE3301** **Module Name: Analog Electronics**

**[Three Hours]**

[Answer **all questions**, each question carries ten marks]

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Q1 Biasing in BJT circuits ensures a stable operating point (Q-point) despite variations in temperature and device parameters. It enables proper operation in the active region for amplification. Techniques such as voltage divider bias and configurations like the Darlington pair improve stability, increase current gain, and enhance circuit performance

a) Explain how a Bipolar Junction Transistor (BJT) amplifier in a common-emitter configuration can be stabilized using small-signal performance analysis.

[1.0 Mark]

b) The Si BJT amplifier circuit shown in Figure Q1.b is a well-stabilized amplifier. Given that the current gain of the transistor is $\beta$ = 175 and the capacitive reactance are negligible at the frequency of operation.
$V_{CC}$ = 10 *V*, $R_1$ = 18 *kΩ*, $R_2$ = 51 *kΩ*, $R_C$ = 4.7 *kΩ*, $R_E$ = 470 *Ω*, $R_L$ = 470 *Ω*, $C_1$=1 *μF* and $C_2$=10 *μF*

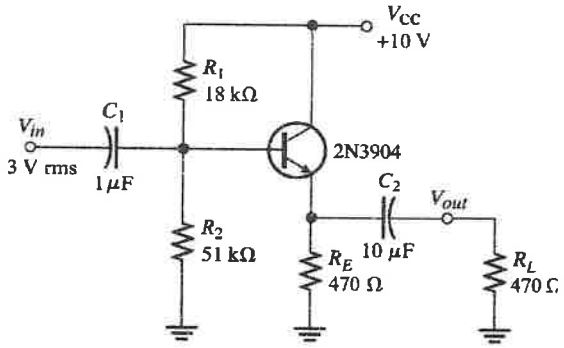


Figure Q1.b

i. Determine the total input resistance of the circuit.
ii. Calculate the voltage gain ($A_v$) of the circuit given in Figure Q1.b.
iii. Calculate the resultant power gain (Ap) considering the power delivered to the load resistance $R_L$.

[4.0 Marks]

c) Figure Q1.c illustrates a transistor amplifier in a common-emitter (CE) configuration.
$V_{CC}$ = 20 *V*, $R_1$ = 22 *kΩ*, $R_2$ = 22 *kΩ*, $R_C$ = 2.2 *kΩ*, $R_E$ = 1 *kΩ*, and $R_L$ = 4.7 *kΩ*
The h-parameters of the transistor are provided as follows:
$h_{ie}$ = 1.6 *kΩ*, $h_{oe}$ = 25 *μS*, $h_{fe}$ = 80 and $h_{re}$ is negligible.

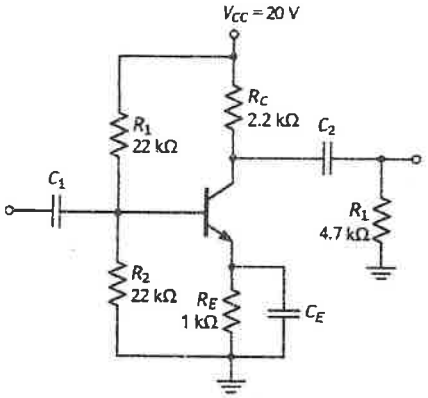


Figure Q1.c

i. Draw the complete small signal analysis circuit for Figure Q1.c using hybrid parameter model.

ii. Show that voltage gain($A_v$) can be given as below. Clearly state all assumptions made in the derivation.

$$A_v = -\left(\frac{h_{fe}}{h_{ie}}\right)\left(R_C \parallel R_L \parallel \frac{1}{h_{oe}}\right)$$

iii. Calculate voltage gain($A_v$) for the circuit given in Figure Q1.c.

[5.0 Marks]

Q2 a) Integrated Circuit (IC) biasing ensures stable operation of transistors under variations in temperature and supply conditions. It establishes consistent operating points and improves circuit performance. Techniques such as current mirrors are commonly used to achieve accurate and stable biasing.

i. Explain why resistor biasing failed in ICs.

ii. Define the compliance voltage effect in a BJT current mirror circuit.

iii.

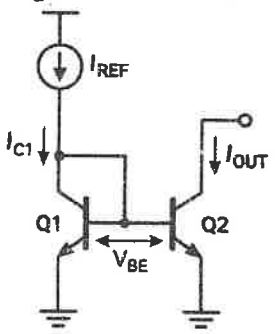


Figure Q2.a

In the active region, the BJT exponential current relationship is given as:

$$I_C = I_S\, e^{\frac{V_{BE}}{V_T}}$$

Where:

$I_C$–Collector current.

$I_S$– Reverse saturation current (scale current).

$V_{BE}$– Base-emitter voltage.

$V_T$– Thermal voltage (26 mV at room temperature).

Using the BJT exponential current relationship, show that $I_{REF} = I_{OUT}$ for the circuit in Figure Q2.a. Clearly state and justify all assumptions made.

[5.0 Marks]

b) An N-channel JFET amplifier circuit is shown in Figure Q2.b. The circuit parameters are as follows: $V_{DD} = 16\ V$, $R_D = 1.0\ k\Omega$, $I_{DSS} = 18\ mA$, $V_P = -6\ V$, $V_{GS} = -2\ V$

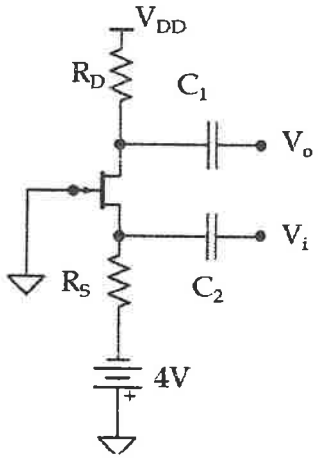


Figure Q2.b

i. Draw the DC equivalent circuit of the N-channel JFET amplifier shown in Figure Q2.b.
ii. Calculate the drain current $I_D$.
iii. Calculate the source voltage $V_S$.
iv. Calculate the source resistance $R_S$.
v. Calculate the drain-to-source voltage $V_{DS}$.
vi. Prove that the N-channel JFET circuit shown in Figure Q2.b operates as an amplifier.

[5.0 Marks]

Q3 a) Figure Q3.a shows a voltage-divider bias enhancement MOSFET circuit, which is intended to operate as an amplifier. The circuit parameters are as follows: $V_{DD} = 18\ V$, $V_T = 2$ V, $I_D = 1.93$ mA, $R_1 = 4.7\ M\Omega$, $R_2 = 2.2$ M$\Omega$, $R_{D1} = 2.2$ k$\Omega$, $R_{S1} = 500\ \Omega$ and $g_m = 1.4\ mS$.

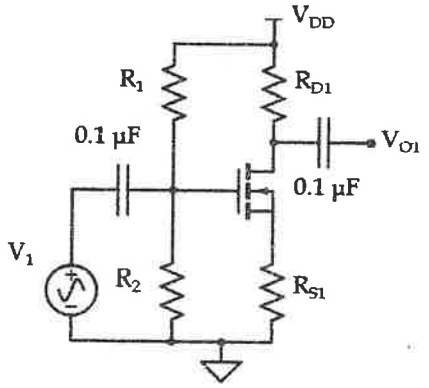


Figure Q3.a

i. Draw the DC analysis equivalent circuit for the circuit shown in Figure Q3.a.
ii. Prove that the circuit shown in Figure Q3.a operates as an amplifier.
iii. Draw the small-signal equivalent circuit of the MOSFET amplifier shown in Figure Q3.a, neglecting the drain resistance.

iv. Prove that the voltage gain ($A_{V1}$) of the MOSFET amplifier shown in Figure Q3.a is given by:

$$A_{V1} = \frac{-g_m \times R_D}{1 + g_m \times R_S}$$

v. Calculate the voltage gain ($A_{V1}$).

[5.0 Marks]

b) Refer to Figure Q3.b. A depletion-mode MOSFET amplifier operates in the saturation region. The circuit parameters are as follows: $V_{DD}$ = 18 $V$, $V_{GS}$ = - 1 V, $I_{DSS}$ = 10 mA, $R_G$ = 3.3 $M\Omega$, $R_{in}$ = 100 k$\Omega$, $R_{S2}$ = 600 $\Omega$, $R_L$ = 1 $k\Omega$ $V_{DS}$ = 3.375 V and $V_P$ = - 4 V

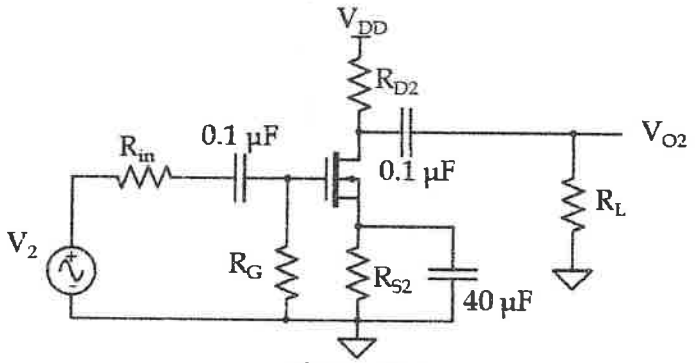


Figure Q3.b

i. Draw the DC analysis equivalent circuit for the circuit shown in Figure Q3.b.

ii. Calculate the drain current ($I_D$) of the MOSFET amplifier shown in Figure Q3.b.

iii. Calculate the resistance $R_{D2}$.

iv. Calculate the transconductance of the depletion-mode MOSFET using the given equation.

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

v. Draw the small-signal equivalent circuit shown in Figure Q3.b, neglecting the drain resistance.

vi. Prove that the voltage gain ($A_{V2}$) of the depletion-mode MOSFET amplifier shown in Figure Q3.b is given by:

$$A_{V2} = \frac{-g_m \times (R_D // R_L) \times R_G}{R_{in} + R_D}$$

vii. Calculate the voltage gain ($A_{V2}$).

[4.0 Marks]

c) When the input voltage is $V_{in}$=10mV, calculate the output voltage ($V_O$) of the circuit shown in Figure Q3.c.

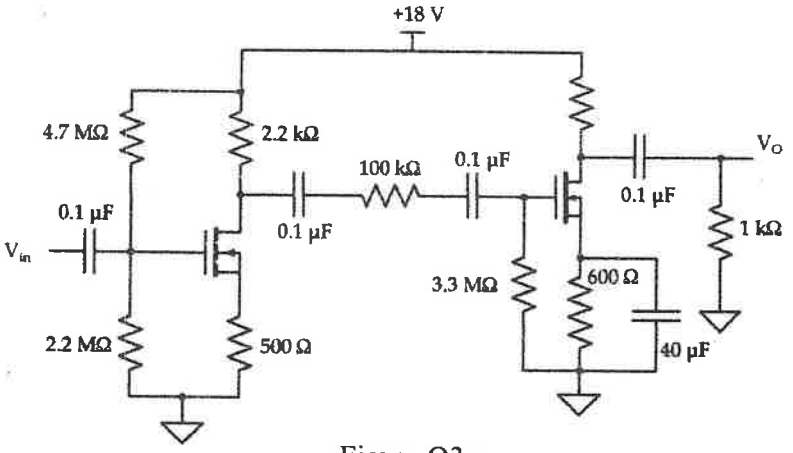


Figure Q3.c

[1.0 Mark]

Q4 a) i. Explain the main difference between an oscillator and a multivibrator.

ii. What are the types of multivibrators? Briefly explain each type.

iii. State the two conditions required for proper operation of an oscillator.

[3.5 Marks]

b) i. Derive the expression for the output voltage of the differential amplifier shown in Figure Q4.b.i, clearly showing all steps and assumptions.

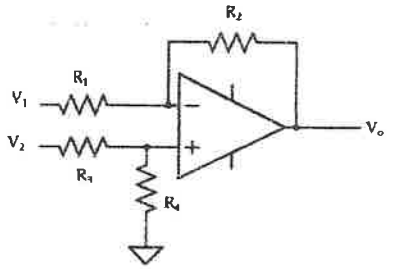


Figure Q4.b.i

ii. Given that $R_2$ = 100 kΩ and $R_3$ = 20 kΩ, calculate the $R_1$ and $R_4$ values of required to obtain an output voltage of

$$V_O = \frac{2}{3}V_2 - V_1$$

Then, redraw the circuit including the calculated component values.

iii. Derive the expression for the output voltage of the inverting amplifier shown in Figure Q4.b.iii.

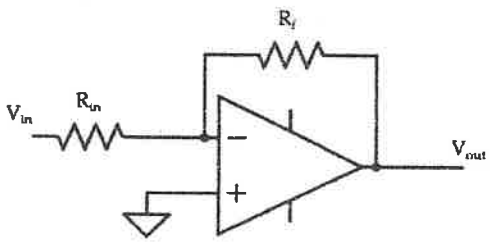


Figure Q4.b.iii

iv. Draw a circuit to obtain the following expression:

$$V_O = \frac{2}{3}V_2 + V_1$$

Clearly specify appropriate component values.

[6.5 Marks]

Q5. A filter is a frequency-selective network that allows desired frequency components to pass while attenuating unwanted signals. In a clap-detection key-tag system, a short-duration impulse-like clap signal with dominant frequency components between **1 kHz and 4 kHz** must be detected accurately. The system is required to pass signals within this frequency range while rejecting low-frequency environmental noise and high-frequency interference.

a) A passive **RLC band-pass filter** is required for a clap-detection key-tag system to pass signals in the frequency range **1 kHz to 4 kHz.**

i. Design a suitable RLC band-pass filter circuit and clearly indicate all components using standard notation

ii. Derive the transfer function $H(s) = \frac{V_o}{V_i}$ of the designed circuit with standard notations.

iii. Sketch the magnitude response of the filter and clearly indicate the lower cutoff frequency($f_L$), upper cutoff frequency($f_H$), and the bandwidth (BW)

iv. Given $f_L = 1$ kHz ,$f_H = 4$ kHz and $R = 10\ k\Omega$, determine the required values of L and C

v. Calculate the resonant frequency($f_r$) of the filter.

[4.0 Marks]

b) To improve selectivity and provide gain, the passive filter is replaced with an **active band-pass filter** using an operational amplifier, as shown in Figure Q5.b.

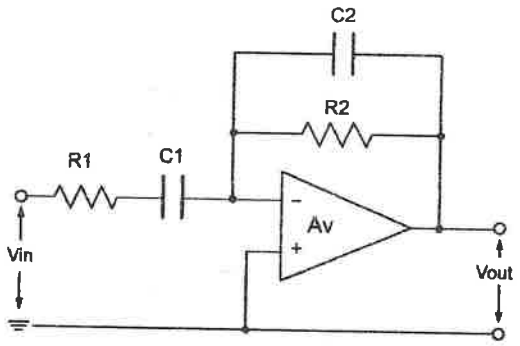


Figure Q5.b

i. Show that the transfer function of the circuit can be expressed as:

$$H(s) = -\frac{sR_2C_1}{1 + s(R_1C_1 + R_2C_2) + s^2R_1R_2C_1C_2}$$

ii. Given $R_1 = R_2 = 1\ \text{k}\Omega$, determine the values of $C_1$and $C_2$to achieve lower and upper cutoff frequencies of 1 kHz and 4 kHz, respectively.

iii. Determine the quality factor (Q) of the filter and comment on its selectivity.

[4.0 Marks]

c)

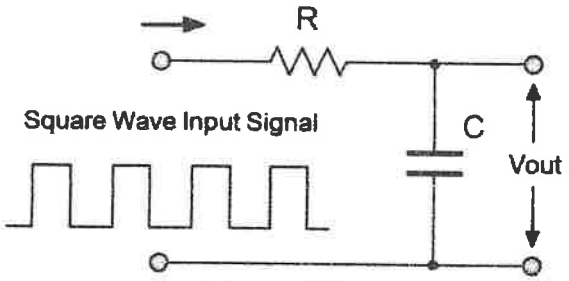


Figure Q5.c

A first-order RC low-pass filter with cutoff frequency $f_c$ is excited by a square wave input signal of frequency $f$, as shown in Figure Q5.c. Sketch the corresponding output waveforms and justify your answers based on the frequency response of the filter.

i. $f \ll fc$

ii. $f \approx fc$

iii. $f \gg fc$

[2.0 Marks]