UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 2 Examination in Engineering: March 2026

Module Number: EE2201 **Module Name: Fundamentals of Electronics (C-23)**

[Three Hours]

[Answer **all questions**, all MCQs carry equal marks]
[Mark your answers in the given answer sheet]

Type A

Section A

1 Select the **correct** term regarding the band gap between conduction and valence bands of a conductor.

a) High b) Low c) None (overlap) d) Moderate

2 Select the **incorrect** statement regarding Extrinsic Semiconductors.

a) In an N-type semiconductor Fermi Level moves up from the middle of the band gap.
b) In a P-type semiconductor Fermi level moves down from the middle of the band gap.
c) In an N-type semiconductor, the probability of an electron occupying the Fermi Level is 50%.
d) In both the N and P-type semiconductors Fermi Level remains at the middle of the band gap.

3 Select the **incorrect** statement regarding P-N junction diodes.

a) Applying a positive voltage to P-side and a negative voltage to N-side makes it forward biased.
b) In order to forward bias a P-N junction, electrons should be provided with enough energy to overcome the depletion region.
c) Applying +5 V to P-side and 0 V does not forward bias a P-N junction diode.
d) In a P-N junction diode, barrier voltage arises due to the depletion region.

Questions 4-5 are based on the circuit given in Figure A.1.

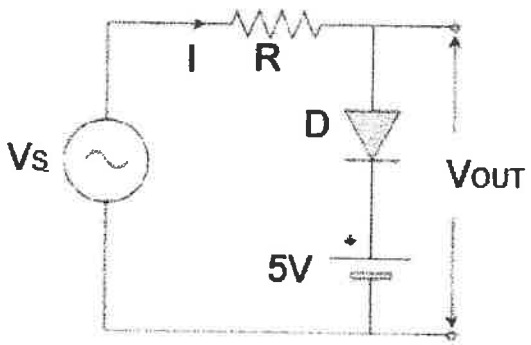


Figure A.1

The voltage source is an AC voltage source in which the output voltage is denoted by Vs and the diode D is an ideal diode (no barrier voltage). The positive peak value of Vs = 7 V.

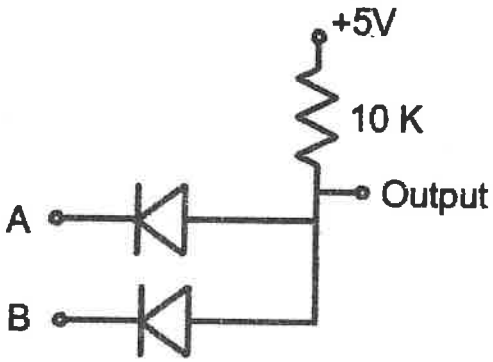
4 Select the circuit based on its functionality.

a) Clipping b) Clamping c) Regulator d) Rectifier

5 Select the **incorrect** voltage combination belong to the circuit.

a) Vs = 3 V, Vout = 3 V
b) Vs = 5 V, Vout = 5 V
c) Vs = 7 V, Vout = 5 V
d) Vs = 7 V, Vout = 5.7 V

6 The inputs A and B of the circuit given in Figure A.2 and B can be either +5 V or 0 V. Select the logic gate implemented by the circuit.



Hint: Apply possible values to A and B and obtain the truth table.

a) OR
b) AND
c) NAND
d) XOR

Figure A.2

7 Select the type of material used in Solar Cells.

a) Regular conductors b) Intrinsic semiconductors c) Extrinsic semiconductors d) Super conductors

Section B

Questions 1 – 5 will be based on Figure B.1.

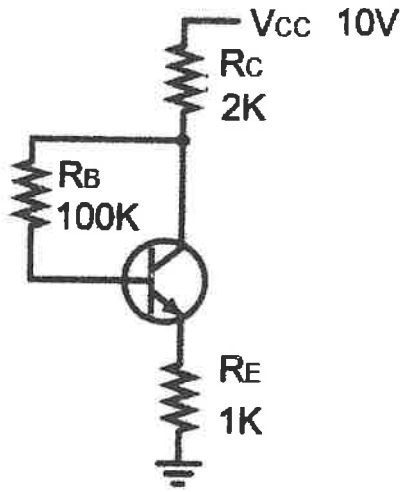


Figure B.1

The voltage gain, β, of the transistor is 100 and V_{BE}, V_{CE}, and V_{BC} has their usual meanings.

1 Identify the type of the transistor used in the circuit.

a) Intrinsic BJT b) NPN BJT c) PNP BJT d) PNP FET

2 Select the **correct** equation to calculate the collector current.

a) $I_C = V_{CC}/(R_C + R_E/\beta)$
b) $I_C = (V_{CC} - V_{CE})/R_C$
c) $I_C = V_{CC}/(R_C + R_E)$
d) $I_C = \beta \cdot (V_{CC} - V_{BE}) / ((\beta+1) \cdot (R_C + R_E) + R_B)$

3 Assuming that the transistor is Silicon-based, select the appropriate value for the V_{CE}.

a) 5.386 V b) 2.330 V c) 2.356 V d) 3.054 V

4 Select the pair of voltages used in identifying the mode of operation of the transistor.

a) V_{CB} and V_{BE} b) V_{CE} and V_{BE} c) V_C and V_E d) V_{CC} and V_{BE}

5 Select the **correct** statement regarding the behavior of the circuit when V_{CC} is increased from 10 V to 30 V.

a) V_{CE} increases and transistor moves to Saturation Mode from Active Mode.

b) V_{CE} increases and transistor remains in Saturation Mode.

c) V_{CE} increases and transistor remains in Active Mode.

d) V_{CE} increases and transistor moves to Active Mode from Saturation Mode.

Question 6-8 are based on Figure B.2.

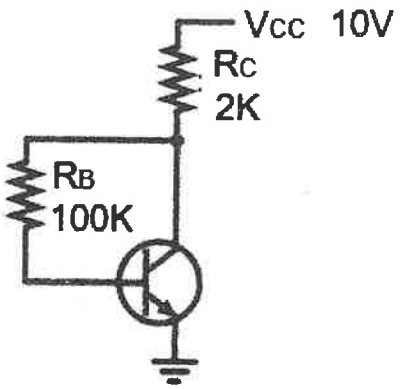


Figure B.2

Suppose that R_E is removed from the circuit in Figure B.1 such that the Emitter of the transistor is directly connected to the ground terminal as shown in Figure B.2. Assume that the transistor is operating in its Active Mode.

The collector voltage is denoted as Vc.

6 Select the **correct** equation for Collector voltage, V_C.

a) $V_C = V_{CC} - R_C \cdot (1+\beta) \cdot V_{CC} / (R_C \cdot (1+\beta) + R_B)$.

b) $V_C = V_{CC} - R_C \cdot \beta \cdot (V_{CC} - V_{BE}) / (R_C \cdot \beta + R_B)$.

c) $V_C = V_{CC} - R_C \cdot (1+\beta) \cdot (V_{CC} - V_{BE}) / (R_C \cdot (1+\beta) + R_B)$.

d) $V_C = V_{CC} - R_C \cdot \beta \cdot V_{CC} / (R_C \cdot \beta + R_B)$.

7 Select the **correct** statement regarding the behavior of V_C, when V_{CC} is increase.

a) V_C increases with increasing V_{CC}. b) V_C decreases with increasing V_{CC}.

c) V_C Stays constant. d) V_C cannot predict the variation of V_C.

8 Considering the behavior of V_{CE} with increasing V_{CC}, select the correct statement regarding the operation of the transistor.
Hint: Consider the generic output characteristics curve and the fact that $V_E = 0$ V.

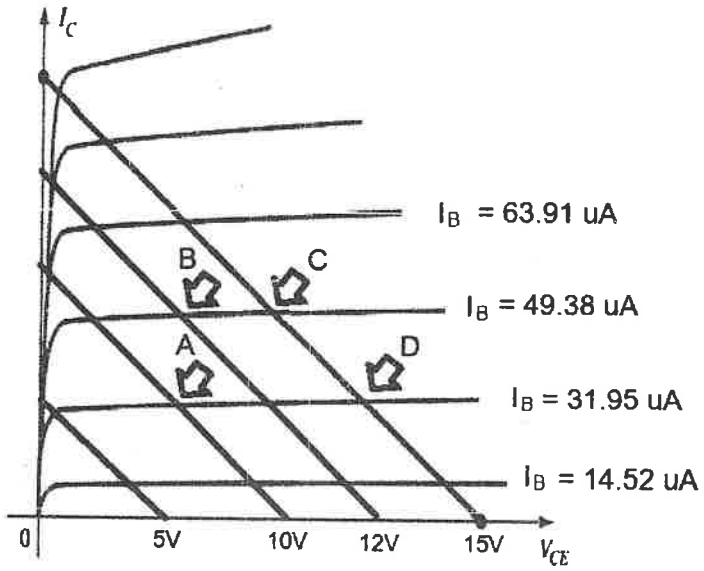
a) The transistor stays in the Active Mode.

b) The transistor moves to the Saturation Mode.

c) The transistor moves to the Cutoff Mode.

d) Cannot predict its behavior from the given information.

9 Considering the DC load lines given in Figure B.3. Identify the valid operating points for the circuit.



a) A and B

b) A and C

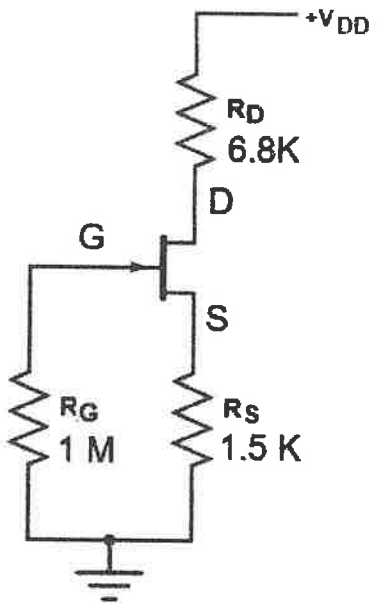
c) B and C

d) B and D

Figure B.3

Section C

Questions 1-4 are based on the circuit given in Figure C.1.



The Pinch-off voltage of the transistor is -3 V, the Saturation Drain Current is 4 mA and V_{DD} = 12 V.

Figure C.1

1 Identify the transistor given in the circuit.

a) N - Channel JFET.

b) P - Channel JFET.

c) N - Channel MOSFET

d) P - Channel MOSFET

2 Select the correct equation. The currents I_D, I_S, and I_G, and voltages V_G, V_{GS} and V_{DS} have their usual meanings.

a) $V_{GS} = - I_D \cdot R_S$

b) $V_{DS} = V_{DD} + I_D \cdot (R_D + R_S)$

c) $V_G = V_{DS} - I_D \cdot R_D$

d) None of the above

3 Select the Drain current, I_D. (*Hint: Solve the quadratic equation.*)

a) 4 mA b) 3 mA c) 2 mA d) 1 mA

4 Suppose that we increased the V_{DD} to 20 V the resultant drain current is 1 mA. Select the correct statement regarding the circuit.

a) The transistor is operating at the Cut-off region since higher V_{DD} reduces Gate control.

b) The Drain current remains at 1 mA as it hardly changes within the Saturation region.

c) The increase in V_{DD} sends the transistor to Ohmic region.

d) Fixed-bias configurations keep the Drain current unchanged.

5 Identify the transistor give in Figure C.2.

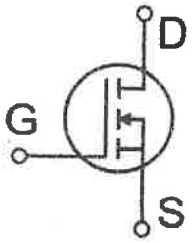


Figure C.2

a) N - Channel Depletion type MOSFET

b) P - Channel Depletion type MOSFET

c) N - Channel Enhancement type MOSFET

d) P - Channel Enhancement type MOSFET

6 If you are to replace only the transistor of the circuit given in Figure C.1 with a MOSFET, why would an N-Channel Depletion-type MOSFET (N-DMOS) is more suitable than an N-Channel Enhancement-type MOSFET (N-EMOS).

a) N-DMOS is normally OFF at V_{GS}=0, while N-EMOS is normally ON.

b) N-DMOS attenuate the input, while N-EMOS amplify the input.

c) N-DMOS conducts current through the channel when V_{GS} is < 0 V, while N-EMOS doesn't.

d) N-DMOS requires positive V_{GS} voltage to turn ON, while N-EMOS requires negative V_{GS}.

7 Select the **incorrect** way of biasing, if we replace the transistor of the circuit given in Figure C.1 with a N-EMOS.

a) Use a voltage divider and connect the Gate between the two resistors in the voltage divider.

b) Connect a large resister from Drain to Gate.

c) Connect a positive voltage source to Gate.

d) Connect the Gate directly to the Ground.

8 Select the reason for CMOS technology being preferred over NMOS or PMOS-only technology in electronic circuits.

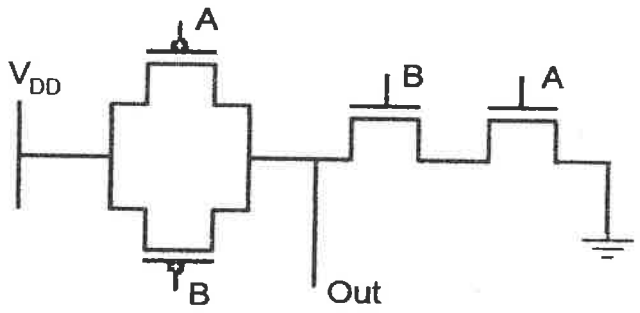
a) Higher switching speed of CMOS.

b) Simpler fabrication process of CMOS.

c) CMOS's better tolerance to high temperatures.

d) Low static power consumption of CMOS.

9 Identity the output of the CMOS circuit given in Figure C.3.



a) A· B

b) A + B

c) $\overline{A \cdot B}$

d) $\overline{A+B}$

Figure C.3

Section D

1 The logic expression $(A + B)\ (A + \bar{B})$ is equivalent to,

a) $\bar{A}$ b) A c) $\bar{B}$ d) B

2 The **minimum** number of NAND gates required to implement 2input XOR function is

a) 3 b) 4 c) 5 d) 6

3 A logic expression is given by $F(A,B,C) = A(B + C) + \bar{A}\,(\bar{B} + \bar{C})$. This expression in **Product of Sum** (POS) form is

a) $\Pi\,(0, 7)$ b) $(A + \bar{B} + \bar{C})(\bar{A} + B + C)$

c) $(A + B + C)(\bar{A} + \bar{B} + \bar{C})$ d) $(\bar{A} + \bar{B} + C)(A + B + \bar{C})$

4 **Minimum** expression obtained when $F(A,B,C,D) = \sum(1,3,4,5,6,7,9,11,12,13,14,15)$ is simplified using a Karnaugh map is given by,

a) $B.D + \bar{B}.\bar{D}$ b) $A.C + \bar{A}.\bar{C}$ c) $B + D$ d) $\bar{A}.C + A.\bar{C}$

5 The logic expression $XYZ + X\bar{Y}Z + XY\bar{Z} + \bar{X}YZ$ is equivalent to

a) $XY + XZ + \bar{Y}\bar{Z}$ b) $X\bar{Y} + Y\bar{Z} + ZX$ c) $XY + (Y + X)Z$ d) $(X + \bar{Y})Z + (Y\bar{Z})$

6 A Combination logic circuit has 3 inputs A, B, and C and one output P. The output goes **high** whenever any two or more inputs are **high**. The output P is given by

a) $A + B + C$ b) ABC c) $A \oplus B \oplus C$ d) $AB + BC + CA$

7 **Minimum expression** obtained when $F(A,B,C,D) = \sum(0,2,5,7,8,10,13,15)$ is simplified using a Karnaugh map is given by

a) $B.D + \bar{B}.\bar{D}$ b) $A.C + \bar{A}.\bar{C}$ c) $B.\bar{D} + \bar{B}.D$ d) $\bar{A}.C + A.\bar{C}$

8 Using a Karnaugh map, the **minimized** form of $f(A,B,C,D) = \Sigma(1,3,5,7,9)$ with don't-care terms $(6, 12, 13)$ is

a) $\bar{A}D + \bar{B}\bar{C}D$ b) $\bar{A}D + \bar{C}D$ c) $\bar{A}C + \bar{C}B$ d) $\bar{A}DC + \bar{B}\bar{C}D$

9 Select the expression which is **not** a rule of Boolean Algebra when X and Y are Boolean variables

a) $X + \bar{X} = 1$ b) $\bar{\bar{X}} = X$ c) $\overline{X+Y} = \bar{X}.\bar{Y}$ d) $X.\bar{X} = 0$

10 The logic expression $\bar{A}\bar{C} + A\bar{C} + BC$ is equivalent to

a) $A + \bar{C}$ b) $B + \bar{C}$ c) $B + C$ d) $A + B$

11 Get an equivalent Boolean expression for the output 'Y' of the digital circuit shown in Figure D.1.

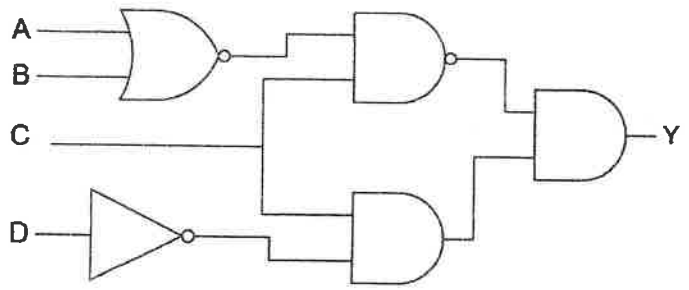


Figure D.1

a) $(A + B + C)\overline{D}$ b) $AC\overline{D} + BC\overline{D}$ c) $\overline{(A + B + C)}\,C\overline{D}$ d) $A\overline{D} + B\bar{C}$

12 A Boolean function is expressed in **Canonical Sum of Products** (SOP) form. What must be true about every product term in this expression?

a) Each term must to simplified to the minimum number of literals possible using Boolean laws.
b) The expression must contain only OR operations between the literals within each term.
c) Each term must contain every literal of the function, either in complemented or uncomplemented form.
d) Every term in the expression must be the complement of a maxterm.

Section E

1 Which of the following is **not True** about sequential circuits?

a) Synchronous sequential circuits share a common clock signal for all flip flops.
b) Asynchronous sequential circuits don't share a common clock signal for all flip flops.
c) In general, synchronous sequential circuits can operate faster than asynchronous sequential circuits.
d) In asynchronous sequential circuits the clock signal is obtained from the output of preceding flip-flop.

2

Table E.1

Q_n	Q_{n+1}	A	B
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

The Table E.1 is the excitation table of

a) a SR Flip flop b) a JK Flip flop
c) a D Flip-flop d) a Toggling flop

3 Which of the following statement about flip-flops and latches is **correct**?

a) Flip-flops are asynchronous, while latches are always synchronous.

b) A latch can store multiple bits, while a flip-flop can store only a single bit.

c) When the clock signal is at logic HIGH, a flip-flop always captures any change in the input data.

d) An asynchronous active-LOW preset sets the flip-flop output to logic '1' when the preset input is '0'.

4 Which of the following statements is **incorrect** about a 3-bit asynchronous binary up counter designed using J-K flip-flops with asynchronous active-low pre-set and clear?

a) At least three negative edge triggered J-K flip-flops are required.

b) All J and K inputs of the flip-flops are tied to logic '1'.

c) The clock frequency of the flip-flop representing the Most Significant Bit (MSB) is twice the clock frequency of the flip-flop representing the Least Significant Bit (LSB).

d) The output of each preceding flip-flop is used as the clock input for the succeeding flip-flop.

5 A student wants to design a **modulo-5 (divide-by-5)** counter using an already designed 3-bit asynchronous binary up counter implemented with J-K flip-flops having asynchronous **active-low** clear and pre-set inputs. Let the flip-flop outputs be $\mathbf{Q_2}$ $\mathbf{Q_1}$, **and** $\mathbf{Q_0}$, where $\mathbf{Q_2}$ represents the MSB and $\mathbf{Q_0}$ represents the LSB. Which Boolean expression represents the **combinational logic** that must be additionally implemented to obtain the modulo-5 operation?

a) $\overline{Q_1 Q_2}$ b) $\overline{Q_0 Q_1}$ c) $\overline{Q_0 Q_1 Q_2}$ d) $\overline{Q_0 Q_2}$

6 The sequential circuit shown Figure E.1 operates as **shift registers**. The states are represented in the order $\mathbf{Q_0}$ $\mathbf{Q_1}$. Assume the **initial state is** $\mathbf{Q_0 Q_1}$ = 00. Which of the following represents the **correct sequence of states** starting from the initial state **after four clock cycles**? *(Hint: Consider the operation of shift registers.)*

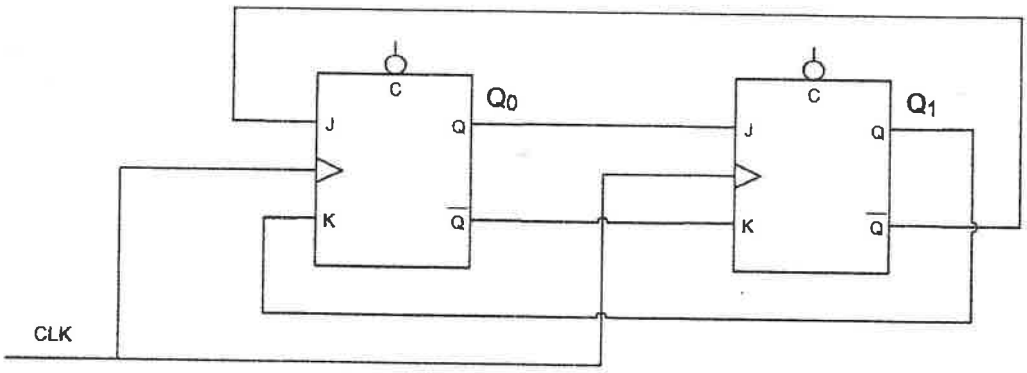


Figure E.1

a) 00, 01, 10, 11, 00 b) 00, 11, 10, 01, 00

c) 00, 10, 11, 01, 00 d) 00, 10, 01, 11, 00

7 For the reliable operation of the synchronous sequential circuit shown in Figure E.1, the clock cycle time of the operating clock must be greater than or equal to the propagation delay of any of the flip-flops in the circuit. If the propagation delay of each flip-flop is 20 ns, identify the **maximum clock frequency** that can be applied to the circuit?

a) 25 MHz b) 50 MHz c) 75 MHz d) 100 MHz

Section F

1 Let A and B be two 2-bit binary numbers represented as A_1A_0 and B_1B_0, respectively. A_1 and $B_1$are the MSBs and A_0 and B_0 are the LSBs. The Boolean expression that gives a logic value **HIGH** when $\boldsymbol{A > B}$ is

a) $A_1\overline{B_1} + (A_0\overline{B_0})$ b) $A_1\overline{B_1} + (A_0\overline{B_0})\overline{(A_1 \oplus B_1)}$

c) $A_0\overline{B_0} + (A_1\overline{B_1})\overline{(A_0 \oplus B_0)}$ d) $A_0\overline{B_0} + (A_1\overline{B_1})(A_0 \oplus B_0)$

2 A 1 - 4 Demultiplexer can also be used as a

a) 2 – 4 Decoder b) 4:2 encoder c) Full adder d) 4:1 Multiplexer

3 If the inputs of a Half-adder are given by X and Y, the Sum(S) and Carry(C) outputs are given by respectively,

a) $X + Y,\ X.Y$ b) $X \oplus Y, \overline{XY}$ c) $X \oplus Y,\ XY$ d) $\overline{X \oplus Y}, XY$

4 A Full adder which adds 3-bits together can be implemented using,

a) Two half-adders b) Two half-adders and one XOR gate

c) Two half-adders and one OR gate d) Two half -adders and one AND gate

5 When AB = 01 and CD = 10 in Figure F.1, which of the following is **true**?

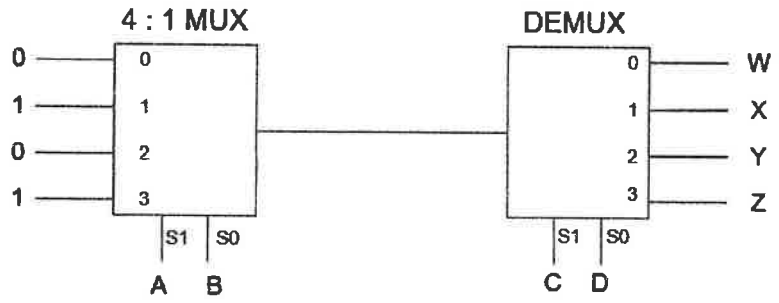


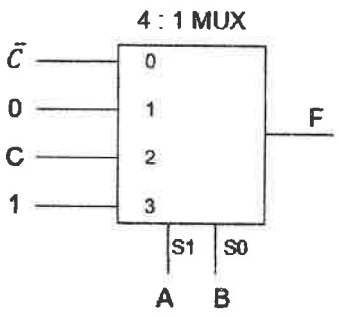
Figure F.1

a) W = 0, X = 1, Y= 0, Z = 1 b) W = 0, X = 0, Y = 0, Z = 1

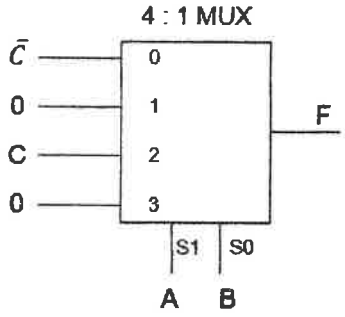
c) W = 1, X = 1, Y = 1, Z = 1 d) W = 0, X = 0, Y = 1, Z = 0

6 Identify the correct implementation of the logic expression $F = \bar{A}.\bar{B}.\bar{C} + A.B.\bar{C} + A.\bar{B}.C$ using a 4:1 Mux.

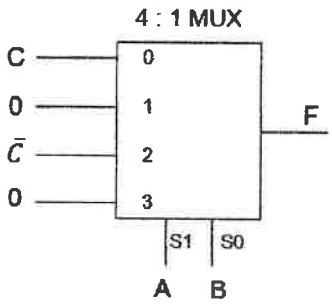
a)



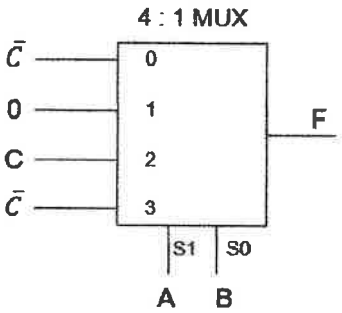
b)



c)



d)



- End of Question Paper -

Use the following equation if necessary

Shockley's equation $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$