UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5, Examination in Engineering: March 2026

Module No: EE5210 Module Name: Hardware Description Language (C-23)

[Two hours]

[Answer **all questions**, each question carries 10 marks]

Q1 a) Consider the following SystemVerilog module

```
module TTL_74LS138 (    input  logic   a, b,   c,
                        input  logic   g1, g2a, g2b,
                        output logic   [7:0] y_n          );
    always_comb begin
        logic [2:0] select;
        select = {c, b, a};

        if ((g1 == 1'b1) && (g2a == 1'b0) && (g2b == 1'b0)) begin
            case (select)
                3'b000:  y_n = 8'b1111_1110;
                3'b001:  y_n = 8'b1111_1101;
                3'b010:  y_n = 8'b1111_1011;
                3'b011:  y_n = 8'b1111_0111;
                3'b100:  y_n = 8'b1110_1111;
                3'b101:  y_n = 8'b1101_1111;
                3'b110:  y_n = 8'b1011_1111;
                3'b111:  y_n = 8'b0111_1111;
                default: y_n = 8'b1111_1111;
            endcase
        end else begin
            y_n = 8'b1111_1111;
        end
    end
endmodule
```

i) Write the *truth table* for the digital circuit, implemented by the module TTL_74LS138(..). Use symbols *X*, *H* and *L* to indicate the logic states *Undefined/Irrelevant*, *High* and *Low*, respectively.

ii) Write a *testbench* to verify the functional accuracy of TTL_74LS138(..)?

[5 Marks]

b) Numerate and briefly describe the primary stages of the design flow for FPGA-based circuit design.

[5 Marks]

Q2 a) Explain the functionality of sequential logic circuit (module) named CTRL(..), in terms of inputs and output of the module. Assume that the input CLK is assigned the system clock of 100MHz, RST_N is assigned the system-wide hardware reset signal (active low), and DUTY_CYCLE can be set to a value within the range of 0 to 100.

```
module CTRL(
    input  logic CLK,                  // 100MHz Input Clock
    input  logic RST_N,                // Active-low asynchronous reset
    input  logic [6:0] DUTY_CYCLE,     // Duty cycle input (0 to 100)
    output logic POUT                  // Periperal output signal
);

    logic [16:0] counter;
    logic [16:0] threshold;

    assign threshold = DUTY_CYCLE * 17'd1000;

    always_ff @(posedge CLK or negedge RST_N)
    begin
        if (!RST_N)
        begin
            counter <= 17'd0;
            POUT <= 1'b0;
        end
        else begin
            if (counter >= 17'd99_999) begin
                counter <= 17'd0;
            end
            else begin
                counter <= counter + 1'b1;
            end

            POUT <= (counter < threshold);
        end
    end

endmodule
```

[5 Marks]

b) The shaft speed of a specific DC motor is measured using an encoder that produces 60 pulses per revolution. Write a module that monitors the encoder input and calculates the motor's speed in RPM (revolutions per minute). The motor has a maximum speed of 2400 RPM.

[5 Marks]

Q3 a) SystemVerilog implementations of Finite State Machines (FSMs) are typically structured using three distinct blocks: Sequential Logic (State Register), Next State Logic, and Output Logic. Draw two separate block diagrams illustrating the signal flow through these elements for a

i) Moore-type Finite State Machine, and

ii) Mealy-type Finite State Machine.

Clearly label all internal signals and input/output paths for both architectures.

[3 Marks]

b) Draw the Mealy and Moore type state transition diagrams for a 1011 sequence detector with overlapping.

[3 Marks]

c) Write a SystemVerilog module named DETECTOR_1011_MEALY(..) that implements the Mealy type 1011 sequence detector.

[4 Marks]

Q4 a) Consider statement **assign** y = {4{a}} & 4'b1010;. If a = 1'b1, what is the hexadecimal value of y?

[2 Marks]

b) What does the value 4'b1Z0X represent in a simulation?

[2 Marks]

c) Explain the fundamental differences between *synchronous reset* and *asynchronous reset* in digital logic design. Support your explanation with appropriate SystemVerilog code snippets (with **always_ff**) as examples for each reset type.

[2 Marks]

d) Assume you are given is a 4-to-1 Multiplexer with inputs D_0, D_1, D_2, D_3, select lines S_1, S_0 and the output Y. Write a *single* line of SystemVerilog code using the conditional operator (? :) to assign MUX output to Y.
Note: The ternary operator is used as y = a?b:c;, which sets y = b if a is true. Otherwise y=c, where a, b, c are SystemVerilog expressions.

[2 Marks]

e) Draw the minimal architecture of a Configurable Logic Block (CLB) as found in a typical FPGA. Your diagram must clearly indicate the signal flow through the following components: Look-up Table (LUT), Flip-Flop (FF) and Multiplexer (MUX).

[2 Marks]