University of Ruhuna- Faculty of Technology

Bachelor of Engineering Technology Honours Degree
Level 4 (Semester II) Examination, December 2025
Academic year 2023/2024

Course Unit: ENT 4212 Programmable Digital Electronics (Written) **Duration: 2 hours**

Instructions for candidates of the question paper.

- Answer all four (04) questions.
- Each question carries twenty-five (25) marks.
- This is a closed-book examination. All written and printed materials, as well as electronics devices including laptops and mobile phones, are not allowed during the examination.
- All symbols and abbreviations have their usual meaning.
- Clearly state all the assumptions you made.

1.

a) Briefly explain the term **Universal Logic Gate** and provide two (02) examples.

(4 marks)

b)

I. Identify the two (02) types of power dissipation in electronic circuits.

(2 marks)

II. A standard TTL (Transistor-Transistor Logic) NOR gate operates at a supply voltage V_{CC} of $5\ V$ and has current drain values of high-level supply current $(I_{CCH}) = 0.8\ mA$ and low-level supply current $(I_{CCL}) = 2.5\ mA$. Calculate the power dissipation of an IC containing six NOR gates when the outputs are at either High or Low state.

(4 marks)

c) A digital logic device has the following voltage characteristics.

- Output high voltage, $V_{OH} = 4.2\ V$
- Input high voltage, $V_{IH} = 3.5\ V$
- Output low voltage, $V_{OL} = 1.3\ V$
- Input low voltage, $V_{IL} = 1.8\ V$

Evaluate whether this device can be used for a combinational logic circuit with a noise margin of $0.6\ V$. (Justify your answer with calculation).

(4 marks)

d) It is required to design a digital control system for a smart patient bed in a hospital. The system operates according to the following specifications. The following Sensors are used to monitor the condition of the patient.

- Pressure (P)
- Body Temperature (T)
- Pulse rate (R)
- Movement (M)

Each sensor output is logic "**1**" when the corresponding parameter exceeds its normal limit and logic "**0**" when it is within the normal range.

The system must satisfy the following conditions.

- If any one of the parameters exceeds its normal limit, a notification must be sent to the nurse.
- If pressure (P) and movement (M) both exceed their limits, the bed adjustment motor should activate automatically.

I. Identify all inputs and outputs of the system and construct a complete truth table that shows all possible input combinations and their corresponding outputs.

(4 marks)

II. Using the truth table from Part I, draw the Karnaugh maps (K-maps) for both outputs, and simplify each using the sum of products (SOP) method.

(4 marks)

III. Draw the logic circuit diagrams for simplified SOP expressions obtained in Part II.

(3 marks)

2.

a)

I. Identify the logic family and list two (02) disadvantages of the combinational digital circuit shown in Figure 1.

(4 marks)

II. Determine the truth table for output logic (V_O).

(3 marks)

III. Considering the circuit shown in Figure 1, briefly explain why the diodes D_1, D_2, and D_3 become forward biased before the diodes D_4 and D_5 when any of the input signals are at a logic Low level. (4 marks)

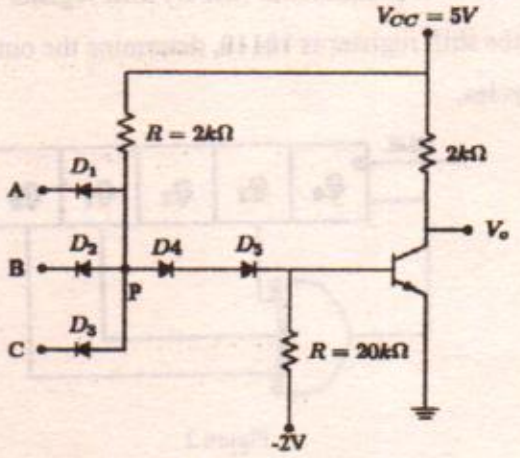

Figure 1

b) State two (02) advantages of CMOS (Complementary Metal-Oxide-Semiconductor) logic family compared to the TTL logic family. (4 marks)

c) Identify the types of MOS (Metal-Oxide-Semiconductor) transistors used in the pull-up and pull-down networks of CMOS logic circuits and briefly explain the reason for using each transistor type in the respective network. (4 marks)

d) Draw the minimum CMOS transistor network that implements the functionality of the Boolean equation $F = \overline{A} + \overline{B}C$. You may assume that both the original and complemented versions of each input variable are available as inputs to the gates.

(6 marks)

3.

a) Identify the two (02) types of data loading mechanisms in digital registers based on the characteristics of the clock (CLK) signal and the timing/control signals.

(2 marks)

b)

I. List the four (04) types of shift registers based on their input and output configurations. (4 marks)

II. Identify the type of shift register that is used to convert serial data from a sensor into parallel form suitable for processing. (1 mark)

III. Identify the type of shift register that allows all bits to be loaded simultaneously and read all bits simultaneously. (1 mark)

IV. A 5-bit Serial-In Parallel-Out (SIPO) shift register is shown in Figure 2. If the initial data of the shift register is **10110**, determine the output of the shift register after three clock cycles. (3 marks)

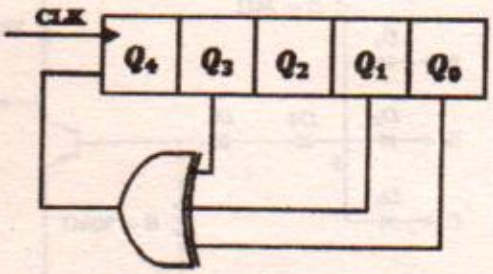

Figure 2

c)

I. Identify three (03) types of simple programmable logic devices (PLDs) commonly used in digital circuit design. (3 marks)

II. Write two (02) advantages of fixed logic devices compared to programmable logic devices. (2 marks)

III. Determine the size of PROM (Programmable Read-Only Memory) required to implement a 4-bit binary adder using only single bit full adders. (3 marks)

d) Consider the following Boolean functions and draw the PAL (Programmable Array Logic) circuit diagram required to implement the given functions using PLDs. (6 marks)

$$F_1(A,B,C) = \sum_m (1,3,4,7)$$

$$F_2(A,B,C) = \sum_m (0,2,6)$$

4.

a)

I. Identify the main difference between an FPGA (Field-Programmable Gate Array) and an ASIC (Application-Specific Integrated Circuit). (3 marks)

II. List two (02) factors that distinguish a hardware description language (HDL) from a conventional programming language. (4 marks)

b) Consider the following input operands and determine the resulting output.

(6 marks)

$$A = 4'b1010; \quad B = 4'b1101; \quad C = 4'b10x1;$$

I. $A * B$ **(Multiplication)**

II. A & C **(Bitwise AND)**

III. A ^~C **(Bitwise XNOR)**

c)

I. Determine the value of Y produced by the following RTL (Resistor-Transistor Logic) code. (3 marks)

```
reg [3:0] X;
reg [3:0] Y;
initial
   begin
      Y = X + 1'bx;
   End
```

II. Analyze the following RTL code and state the output that will be displayed.

(3 marks)

```
reg [11 * 8: 1] name;
initial
   begin
      name = "Hello World";
      $display(Name=%name, name[32:1]);
   end
```

d) Based on the 4-bit full adder shown in Figure 3, write the complete Verilog code to instantiate the corresponding module. (6 marks)

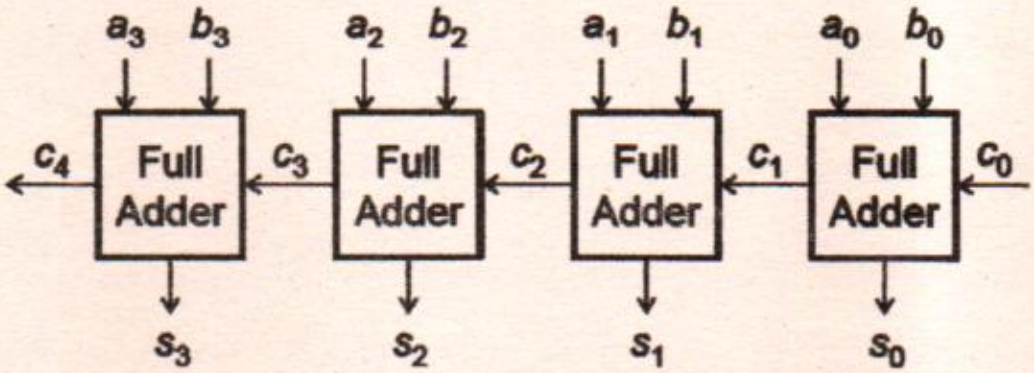

Figure 3

End of Paper